CrossLink-NX Family

Data Sheet

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
ADC	Analog to Digital Converter
BGA	Ball Grid Array
CDR	Clock and Data Recovery
CRC	Cycle Redundancy Code
DCC	Dynamic Clock Control
DCS	Dynamic Clock Select
DDR	Double Data Rate
DLL	Delay Locked Loops
DSP	Digital Signal Processing
DTR	Digital Temperature Readout
EBR	Embedded Block RAM
ECC	Error Correction Coding
ECLK	Edge Clock
FFT	Fast Fourier Transforms
FIFO	First In First Out
FIR	Finite Impulse Response
LC	Logic Cell
LRAM	Large RAM
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVTTL	Low Voltage Transistor-Transistor Logic
LUT	Look Up Table
MLVDS	Multipoint Low-Voltage Differential Signaling
PCI	Peripheral Component Interconnect
PCS	Physical Coding Sublayer
PCLK	Primary Clock
PDPR	Pseudo Dual Port RAM
PFU	Programmable Functional Unit
PIC	Programmable I/O Cells
PLL	Phase Locked Loops
POR	Power On Reset
SER	Soft Error Rate
SEU	Single Event Upset
SLVS	Scalable Low-Voltage Signaling
SPI	Serial Peripheral Interface
SPR	Single Port RAM
SRAM	Static Random-Access Memory
TAP	Test Access Port
TDM	Time Division Multiplexing

1. General Description

CrossLink™-NX family of low-power FPGAs can be used in a wide range of applications, and are optimized for bridging and processing needs in Embedded Vision applications – supporting a variety of high bandwidth sensor and display interfaces, video processing and machine learning inferencing. It is built on Lattice Nexus FPGA platform, using low-power 28 nm FD-SOI technology. It combines the extreme flexibility of an FPGA with the low power and high reliability (due to extremely low SER) of FD-SOI technology, and offers small footprint package options.

CrossLink-NX supports a variety of interfaces including MIPI D-PHY (CSI-2, DSI), LVDS, SLVS, subLVDS, PCI Express (Gen1, Gen2), SGMII (Gigabit Ethernet), and more.

Processing features of CrossLink-NX include up to 39K Logic Cells, 56 18x18 multipliers, 2.9 Mb of embedded memory (consisting of EBR and LRAM blocks), distributed memory, DRAM interfaces (supporting DDR3, DDR3L, LPDDR2, and LPDDR3 up to 1066 Mbps x 16 data width).

CrossLink-NX FPGAs support fast configuration of its reconfigurable SRAM-based logic fabric, and ultra-fast configuration of its programmable sysI/O™. Security features to secure user designs include bitstream encryption and password protection. In addition to the high reliability inherent to FD-SOI technology (due to its extremely low SER), active reliability features such as built-in frame-based SED/SEC (for SRAM-based logic fabric), and ECC (for EBR and LRAM) are also supported. Built-in ADC is available in each device for system monitoring functions.

Lattice Radiant™ design software allows large complex user designs to be efficiently implemented on CrossLink-NX FPGA family. Synthesis library support for CrossLink-NX devices is available for popular logic synthesis tools. Radiant tools use the synthesis tool output along with constraints from its floor planning tools, to place and route the user design in CrossLink-NX device. The tools extract timing from the routing, and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for CrossLink-NX family. By using these configurable soft IP cores as standardized blocks, you are free to concentrate on the unique aspects of your design, increasing your productivity.

1.1. Features

- Programmable Architecture
  - 17K to 39K logic cells
  - 24 to 56 18 x 18 multipliers (in sysDSP™ blocks)
  - 2.5 to 2.9 Mb of embedded memory blocks (EBR, LRAM)
  - 36 to 192 programmable sysI/O (High Performance and Wide Range I/O)
- MIPI D-PHY
  - Up to two hardened 4-lane MIPI D-PHY interfaces
    - Up to eight lanes total
    - Transmit or receive
    - Supports CSI-2, DSI
    - 20 Gbps aggregate bandwidth
    - 2.5 Gbps per lane, 10 Gbps per D-PHY interface
  - Additional Soft D-PHY interfaces supported by High Performance (HP) sysI/O
    - Transmit or receive
    - Supports CSI-2, DSI
    - Up to 1.5 Gbps per lane
- Programmable sysI/O supports wide variety of interfaces
  - High Performance (HP) on bottom I/O dual rank
    - Supports up to 1.8 V V_{CCIO}
    - Mixed voltage support (1.0 V, 1.2 V, 1.5 V, 1.8 V)
    - High-speed differential up to 1.5 Gbps
    - Supports soft D-PHY (Tx/Rx), LVDS 7:1 (Tx/Rx), SLVS (Tx/Rx), subLVDS (Rx)
    - Supports SGMII (Gb Ethernet) – 2 channels (Tx/Rx) at 1.25 Gbps
    - Dedicated DDR3/DDR3L and LPDDR2/LPDDR3 memory support with DQS logic, up to 1066 Mbps data-rate and x16 data-width
  - Wide Range (WR) on Left, Right and Top I/O Banks
    - Supports up to 3.3 V V_{CCIO}
    - Mixed voltage support (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V)
    - Programmable slew rate (slow, med, fast)
    - Controlled impedance mode
    - Emulated LVDS support
    - Hot-socketing

- Power Modes – Low Power versus High-Performance
  - User selectable
  - Low-Power mode for power and/or thermal challenges
  - High-Performance mode for faster processing
- Small footprint package options
  - 4 x 4 mm^2 to 10 x 10 mm^2 package options
- 2x SGMII CDR at up to 1.25 Gbps – to support 2 channels SGMII using HP I/O
  - CDR for RX
  - 8b/10b decoding
  - Independent Loss of Lock (LOL) detector for each CDR block
- sysCLOCK™ analog PLLs
  - Three in 39K LC and two in 17K LC device
  - Six outputs per PLL
  - Fractional N
  - Programmable and dynamic phase control
- sysDSP Enhanced DSP blocks
  - Hardened pre-adder
  - Dynamic Shift for AI/ML support
  - Four 18 x 18, eight 9 x 9, two 18 x 36, or 36 x 36
  - Advanced 18 x 36, two 18 x 18, or four 8 x 8 MAC
- Flexible memory resources
  - Up to 1.5 Mb sysMEM™ Embedded Block RAM (EBR)
  - Programmable width
  - ECC
  - FIFO
  - 80k to 240k bits distributed RAM
  - Large RAM Blocks
    - 0.5 Mbits per block
    - Up to five blocks (2.5 Mb total) per device
- SerDes – PCIe Gen2 x1 channel (Tx/Rx) hard IP in 39K LC device
  - Hard IP supports
    - Gen1, Gen2, Multi-Function, End Point, Root Complex
- Internal bus interface support
  - APB control bus
  - AHB-Lite for data bus
  - AXI4-streaming
- Configuration – Fast, Secure
  - SPI – x1, x2, x4 up to 150 MHz
    - Master and Slave SPI support
  - JTAG
  - I^2C and I3C
  - Ultrafast I/O configuration for instant-on support
  - Less than 15 ms full device configuration for LIFCl-40
  - Bitstream Security
    - Encryption
    - Authentication
- Cryptographic engine
  - Bitstream encryption – using AES-256
  - Bitstream authentication – using ECDSA
  - Hashing algorithms – SHA, HMAC
  - True Random Number Generator
  - AES 128/256 Encryption
- Single Event Upset (SEU) Mitigation Support
  - Extremely low Soft Error Rate (SER) due to FD-SOI technology
  - Soft Error Detect – Embedded hard macro
  - Soft Error Correction – Without stopping user operation
  - Soft Error Injection – Emulate SEU event to debug system error handling
- ADC – 1 MSPS, 12-bit SAR
  - 2 ADCs per device
  - 3 Continuous-time Comparators
  - Simultaneous sampling
- System Level Support
  - IEEE 1149.1 and IEEE 1532 compliant
  - Reveal Logic Analyzer
  - On-chip oscillator for initialization and general use
  - 1.0 V core power supply

Table 1.1. CrossLink-NX Commercial/Industrial Family Selection Guide

Device	LIFCL-17	LIFCL-40
Logic Cells[1]	17K	39K
Embedded Memory (EBR) Blocks (18 Kb)	24	84
Embedded Memory (EBR) Bits (Kb)	432	1,512
Distributed RAM Bits (Kb)	80	240
Large Memory (LRAM) Blocks	5	2
Large Memory (LRAM) Bits (Kb)	2560	1024
18 X 18 Multipliers	24	56
ADC Blocks	2	2
450 MHz High Frequency Oscillator	1	1
128 KHz Low Power Oscillator	1	1
GPLL	2	3
Hardened 10 Gbps D-PHY Quads[2]	2	2
Hardened 2.5 Gbps D-PHY Data Lanes (total)[2]	8	8
PCIe Gen2 Hard IP	—	1
Packages (Size, Ball Pitch)	**D-PHY Quads (D-PHY Data Lanes) / Wide Range (WR) GPIO (Top/Left/Right Banks) / High Performance (HP) GPIOs (Bottom Banks)**	
72 WLSCP (3.8 x 4.1 mm^2, 0.4 mm)	1(4)/15/24	—
72 QFN (10 x 10 mm^2, 0.5 mm)	1(4)/17/22	1(4)/17/22
121 csfBGA (6 x 6 mm^2, 0.5 mm)	2(8)/23/48	2(8)/23/48
256 caBGA (14 x 14 mm^2, 0.8 mm)	2(8)/29/48	2(8)/88/74, PCIe x1
289 csBGA (9.5 x 9.5 mm^2, 0.5 mm)	—	2(8)/105/74, PCIe x1
400 caBGA (17 x 17 mm^2, 0.8 mm)	—	2(8)/117/74, PCIe x1

Notes:

1. Logic Cells = LUTs x 1.2 effectiveness.
2. Additional soft D-PHY Tx/Rx interfaces (at up to 1.5 Gbps per lane) are available using sysI/O.

Table 1.2. CrossLink-NX Automotive Family Selection Guide

Device	LIFCL-17	LIFCL-40
Logic Cells[1]	17K	39K
Embedded Memory (EBR) Blocks (18 Kb)	24	84
Embedded Memory (EBR) Bits (Kb)	432	1,512
Distributed RAM Bits (Kb)	80	240
Large Memory (LRAM) Blocks	5	2
Large Memory (LRAM) Bits (Kb)	2560	1024
18 X 18 Multipliers	24	56
ADC Blocks	2	2
450 MHz High Frequency Oscillator	1	1
128 KHz Low Power Oscillator	1	1
GPLL	2	3
Hardened 10 Gbps D-PHY Quads[2]	2	2
Hardened 2.5 Gbps D-PHY Data Lanes (total)[2]	8	8
PCIe Gen2 Hard IP	—	1

Packages (Size, Ball Pitch)	D-PHY Quads (D-PHY Data Lanes) / Wide Range (WR) GPIO (Top/Left/Right Banks) / High Performance (HP) GPIOs (Bottom Banks)	
121 csfBGA (6 x 6 mm^2, 0.5 mm)	2(8)/23/48	2(8)/23/48
256 caBGA (14 x 14 mm^2, 0.8 mm)	2(8)/29/48	2(8)/88/74, PCIe x1

Notes:

1. Logic Cells = LUTs x 1.2 effectiveness.
2. Additional soft D-PHY Tx/Rx interfaces (at up to 1.5 Gbps per lane) are available using sysI/O.

2. Architecture

2.1. Overview

Each CrossLink-NX device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM Embedded Block RAM (EBR) and rows of sysDSP Digital Signal Processing blocks, as shown in Figure 2.1. The CrossLink-NX-40 devices have two rows of DSP blocks and contain three rows of sysMEM EBR blocks. In addition, CrossLink-NX-40 devices includes two Large SRAM blocks. The sysMEM EBR blocks are large, dedicated 18 Kb fast memory blocks and have built-in ECC and FIFO support. Each sysMEM block can be configured to a single, pseudo dual or true dual port memory in a variety of depths and widths as RAM or ROM. Each DSP block supports variety of multiplier, adder configurations with one 108-bit or two 54-bit accumulators supported, which are the building blocks for complex signal processing capabilities.

Each PIC block encompasses two PIO (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the CrossLink-NX devices are arranged in seven banks allowing the implementation of a wide variety of I/O standards. The Wide Range (WR) I/O banks that are located in the top, left and right sides of the device provide flexible ranges of general purpose I/O configurations up to 3.3 V VCCIOs. The banks located in the bottom side of the device are dedicated to High Performance (HP) interfaces such as LVDS, MIPI, DDR3, LPDDR2, and LPDDR3 supporting up to 1.8 V VCCIOs.

The Programmable Functional Unit (PFU) contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFU block is optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. The registers in PFU and sysI/O blocks in CrossLink-NX devices can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

In addition, CrossLink-NX-40 devices provide various system level hard IP functional and interface blocks such as PCIe, D-PHY, I^2C, SGMII/CDR, and ADC blocks. PCIe hard IP supports PCIe 2.0 and D-PHY supports up to 2.5 Gbps per lane. CrossLink-NX devices also provide security features to help secure user designs and deliver more robust reliability features to the user designs by using enhanced frame-based SED/SEC functions.

Other blocks provided include PLLs, DLLs, and configuration functions. The PLL and DLL blocks are located at the corners of each device. CrossLink-NX devices also include Lattice Memory Mapped Interface (LMMI) which is a Lattice standardized interface for simple read and write operations to support controlling internal IPs.

Every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The CrossLink-NX devices use 1.0 V as their core voltage.

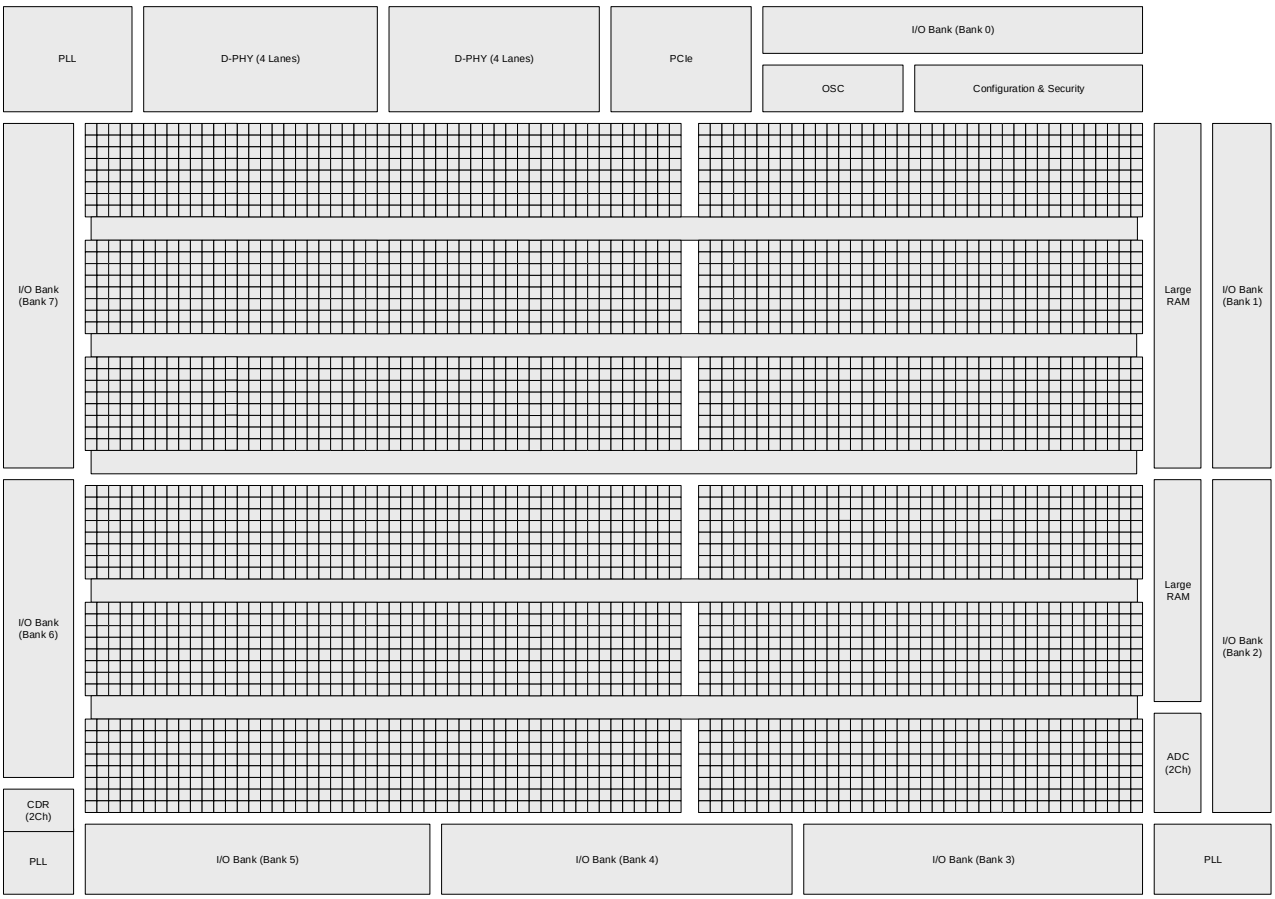


Figure 2.1. Simplified Block Diagram, CrossLink-NX-40 Device (Top Level)

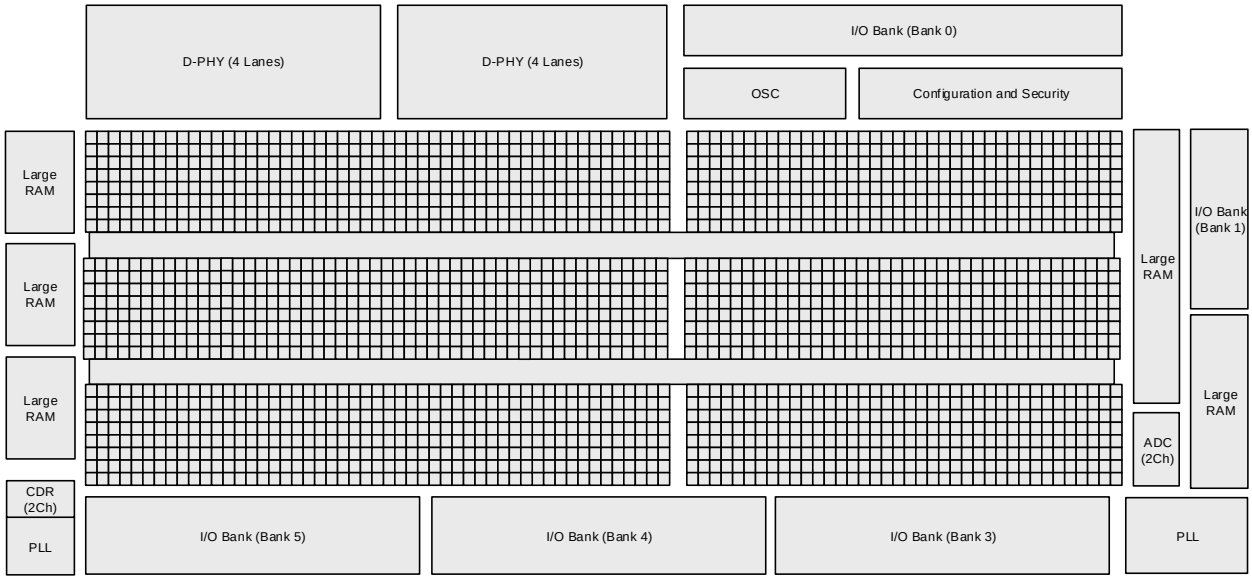


Figure 2.2. Simplified Block Diagram, CrossLink-NX-17 Device (Top Level)

2.2. PFU Blocks

The core of the CrossLink-NX device consists of PFU blocks. Each PFU block consists of four interconnected slices numbered 0-3 as shown in Figure 2.3. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing.

The PFU block can be used in Distributed RAM or ROM function, or used to perform Logic, Arithmetic, or ROM functions. Table 2.1 shows the functions each slice can perform in either mode.

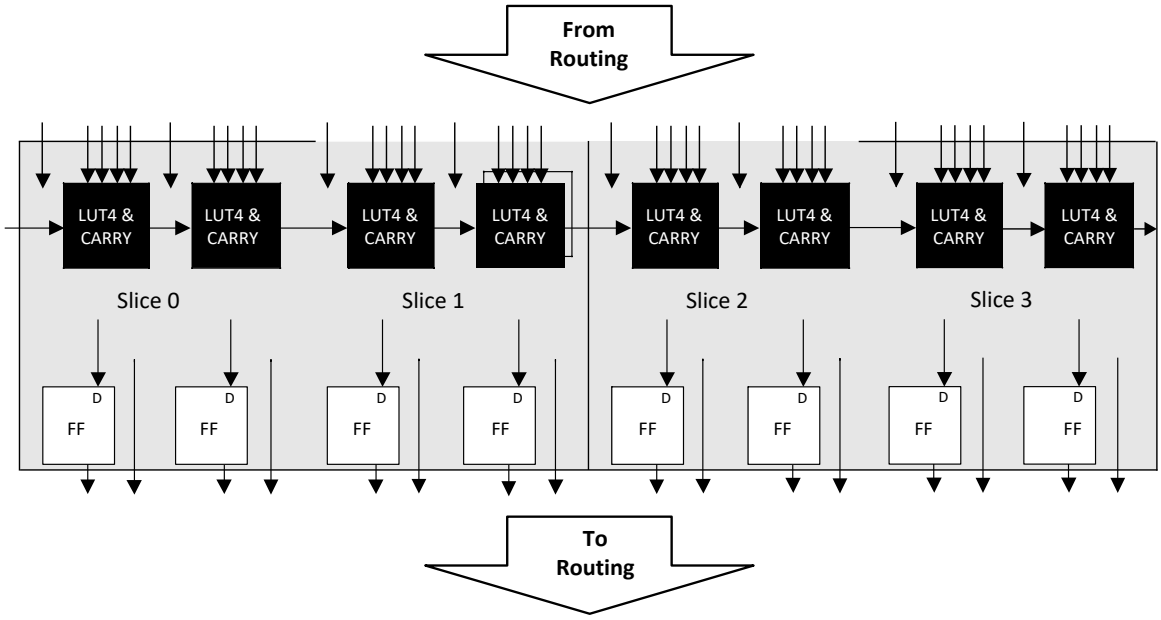


Figure 2.3. PFU Diagram

2.2.1. Slice

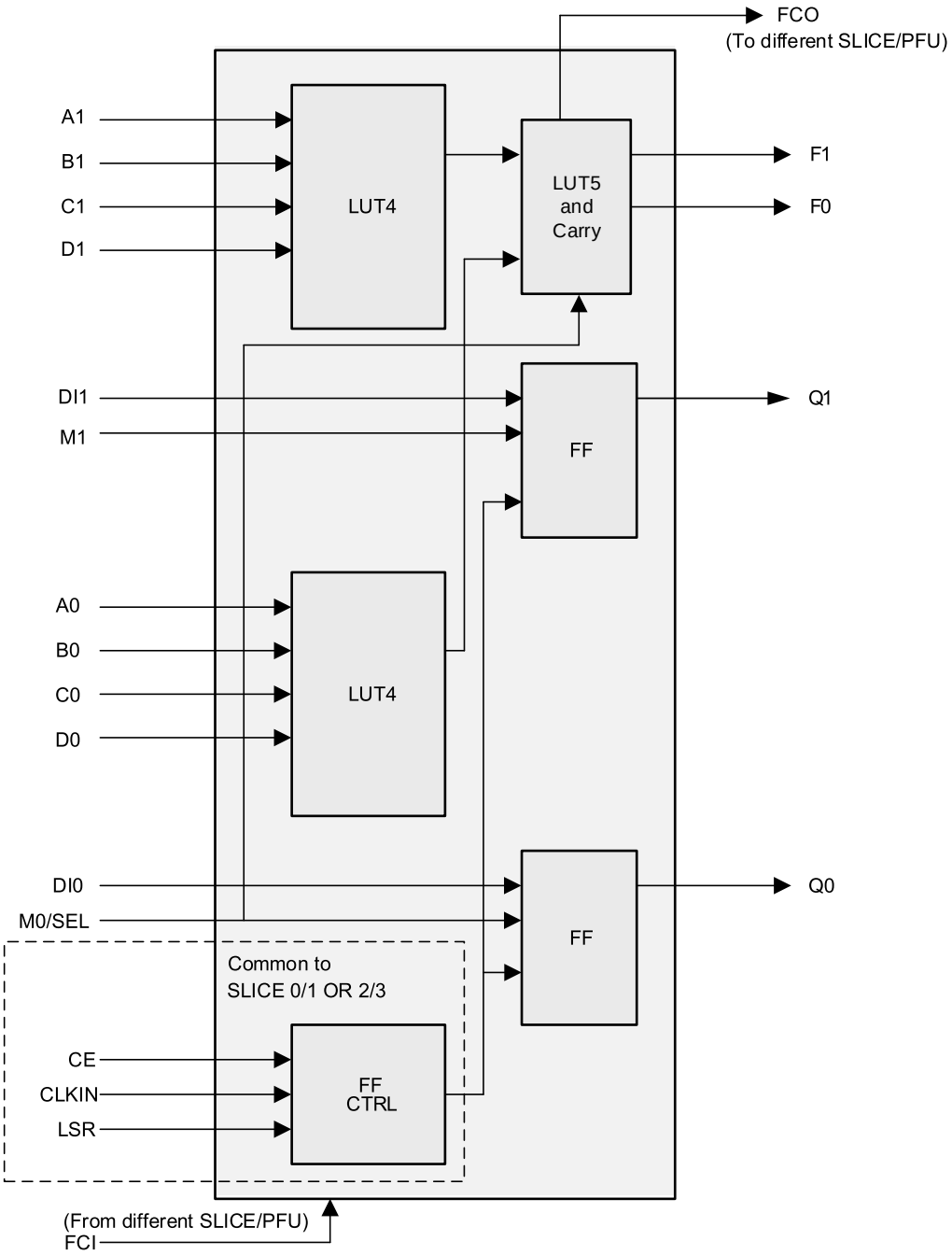
Each slice contains two LUT4s feeding two registers. In Distributed SRAM mode, Slice 0 and Slice 1 are configured as distributed memory, and Slice 2 is not available as it is used to support Slice 0 and Slice 1 while Slice 3 is available as Logic or ROM. Table 2.1 shows the capability of the slices along with the operation modes they enable. In addition, each Slice contains logic that allows the LUTs to be combined to perform a LUT5 function. There is control logic to perform set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select, and wider RAM/ROM functions.

Table 2.1. Resources and Modes Available per Slice

Slice	PFU (Used in Distributed SRAM)		PFU (Not used as Distributed SRAM)	
	Resources	Modes	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 1	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 2	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM

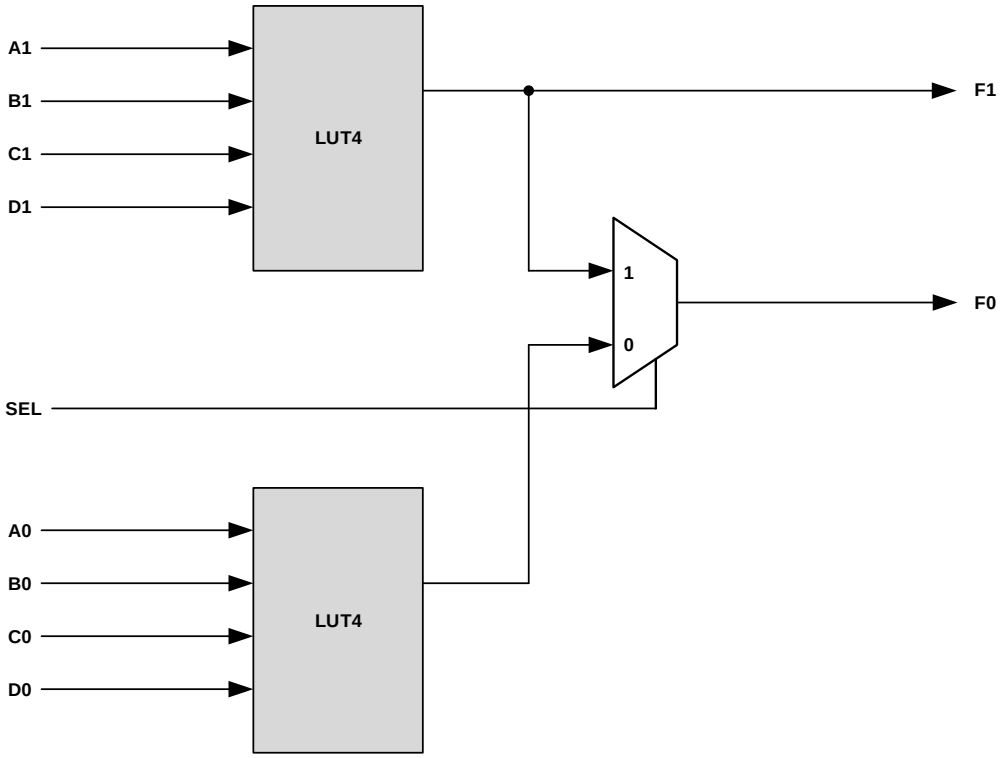
Figure 2.4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative edge trigger.

Each slice has 17 input signals: 16 signals from routing and one from the carry-chain (from the adjacent slice or PFU). Three of them are used for FF control and shared between two slices (0/1 or 2/3). There are five outputs: four to routing and one to carry-chain (to the adjacent PFU). Table 2.2 and Figure 2.4 list the signals associated with all the slices. Figure 2.5 shows the slice signals that support a LUT5 or two LUT5 functions. F0 can be configured to have a LUT4 or LUT5 output while F1 is for a LUT4 output.



*Note: In RAM mode, LUT4s use the following signals:
QWD0/1
QWDN0/1
QWAS00~03, QWAS10~13

Figure 2.4. Slice Diagram



*Note: In RAM mode, LUT4s use the following signals:
QWD0/1
QWDN0/1
QWAS00~03, QWAS10~13

Figure 2.5. Slice Configuration for LUT4 and LUT5

Table 2.2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Data signal	M0, M1	Direct input to FF from fabric
Input	Control signal	SEL	LUT5 mux control input
Input	Data signal	DI0, DI1	Inputs to FF from LUT4 F0/F1 outputs
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLKIN	System Clock
Input	Inter-PFU signal	FCI	Fast Carry-in[1]
Output	Data signals	F0	LUT4/LUT5 output signal
Output	Data signals	F1	LUT4 output signal
Output	Data signals	Q0, Q1	Register outputs
Output	Inter-PFU signal	FCO	Fast carry chain output[1]

Note: See Figure 2.4 for connection details.

2.2.2. Modes of Operation

Slices 0-2 have up to four potential modes of operation: Logic, Ripple, RAM and ROM. Slice 3 is not needed for RAM mode, it can be used in Logic, Ripple, or ROM modes.

2.2.2.1. Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice.

2.2.2.2. Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with asynchronous clear 2-bit using dynamic control
- Up/Down counter with preload (sync) 2-bit using dynamic control
- Comparator functions of A and B inputs 2-bit
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B
- Up/Down counter with A greater-than-or-equal-to B comparator 2-bit using dynamic control
- Up/Down counter with A less-than-or-equal-to B comparator 2-bit using dynamic control
- Multiplier support Ai*Bj+1 + Ai+1*Bj in one logic cell with 2 logic cells per slice
- Serial divider 2-bit mantissa, shift 1bit/cycle
- Serial multiplier 2-bit, shift 1bit/cycle or 2bit/cycle

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

2.2.2.3. RAM Mode

In this mode, a 16 x 4-bit distributed single or pseudo dual port RAM can be constructed in one PFU using each LUT block in Slice 0 and Slice 1 as a 16 x 2-bit memory in each slice. Slice 2 is used to provide memory address and control signals. CrossLink-NX devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software constructs these using distributed memory primitives that represent the capabilities of the PFU. Table 2.3 lists the number of slices required to implement different distributed RAM primitives. For more information about using RAM in CrossLink-NX devices, refer to CrossLink-NX Memory Usage Guide (FPGA-TN-02094).

Table 2.3. Number of Slices Required to Implement Distributed RAM

	SPR 16 X 4	PDPR 16 X 4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

2.2.2.4. ROM Mode

ROM mode uses the LUT logic; hence, Slice 0 through Slice 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, refer to CrossLink-NX Memory Usage Guide (FPGA-TN-02094).

2.3. Routing

There are many resources provided in the CrossLink-NX devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The CrossLink-NX family has an enhanced routing architecture that produces a compact design. The Radiant software tool suites take the output of the synthesis tool and places and routes the design.

2.3.1. Clocking Structure

The CrossLink-NX clocking structure consists of clock synthesis blocks, sysCLOCK PLL; balanced clock tree networks, PCLK and ECLK; and efficient clock logic modules, Clock Dividers (PCLKDIV and ECLKDIV) and Dynamic Clock Select (DCS), Dynamic Clock Control (DCC), and DLL. Each of these functions is described as follow.

2.3.2. Global PLL

The Global PLLs (GPLL) provide the ability to synthesize clock frequencies. The devices in the CrossLink-NX family support two or three full-featured General Purpose GPLLs. The Global PLLs provide the ability to synthesize clock frequencies.

The architecture of the GPLL is shown in Figure 2.6. A description of the GPLL functionality follows.

REFCK is the reference frequency input to the PLL and its source can come from external CLK inputs or from internal routing. The CLKI input feeds into the input Clock Divider block.

CLKFB is the feedback signal to the GPLL which can come from internal feedback path or routing. The feedback divider is used to multiply the reference frequency and thus synthesize a higher or lower frequency clock output.

The PLL has six clock outputs CLKOP, CLKOS, CLKOS2, CLKOS3, CLKOS4, and CLKOS5. Each output has its own output divider, thus allowing the GPLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. Each GPLL output can be used to drive the primary clock or edge clock networks.

The setup and hold times of the device can be improved by programming a phase shift into the output clocks which advances or delays the output clock with reference to the un-shifted output clock. This phase shift can be either programmed during configuration or can be adjusted dynamically using the DIRSEL, DIR, DYNROTATE, and LOADREG ports.

The LOCK signal is asserted when the GPLL determines it has achieved lock and de-asserted if a loss of lock is detected.

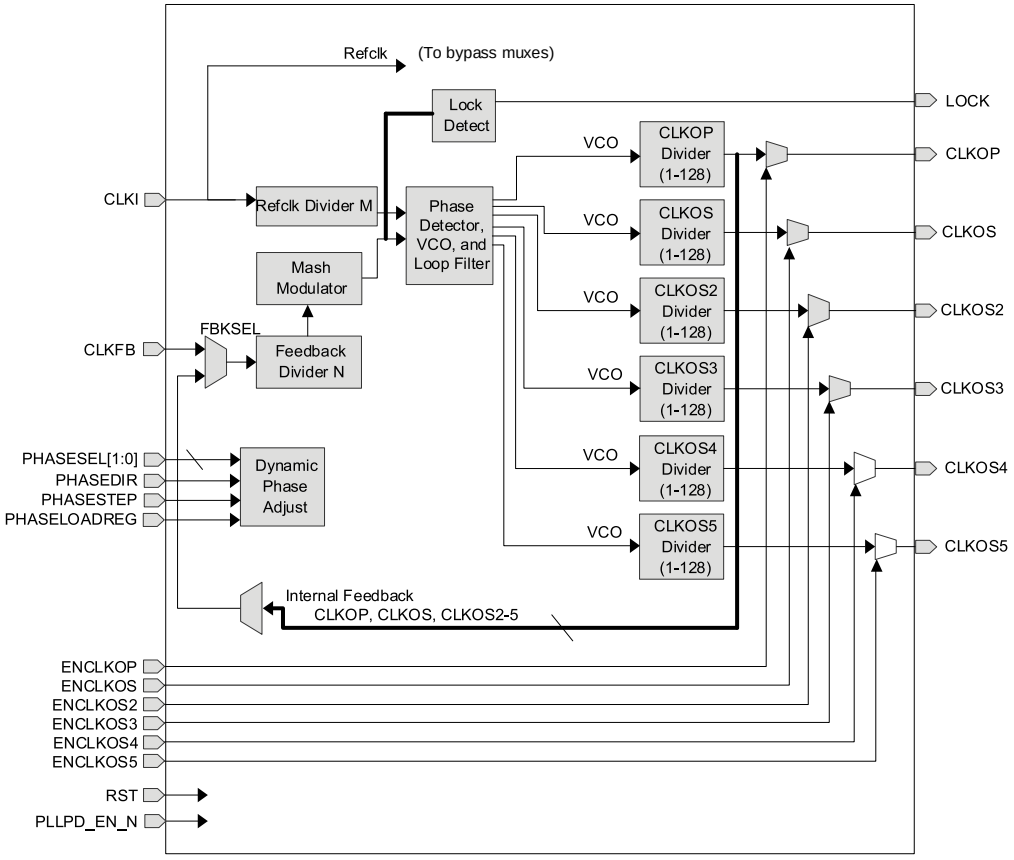


Figure 2.6. General Purpose PLL Diagram

For more details on the PLL, you can refer to the CrossLink-NX sysCLOCK PLL/DLL Design and Usage Guide (FPGA-TN-02095).

2.3.3. Clock Distribution Network

There are two main clock distribution networks for any member of the CrossLink-NX product family, namely Primary Clock (PCLK) and Edge Clock (ECLK). These clock networks can be driven from many different sources, such as Clock Pins, PLL outputs, DLLDEL outputs, Clock divider outputs, SerDes/PCS clocks and user logic. There are clock divider blocks (ECLKDIV and PCLKDIV) to provide a slower clock from these clock sources.

CrossLink-NX supports glitchless Dynamic Clock Control (DCC) for the PCLK Clock to save dynamic power. There are also Dynamic Clock Selection logic to allow glitchless selection between two clocks for the PCLK network (DCS).

Overview of Clocking Network is shown in Figure 2.7 for CrossLink-NX device. The shaded blocks (PCIe and upper left PLL) are not available in the 17K Logic Cell device.

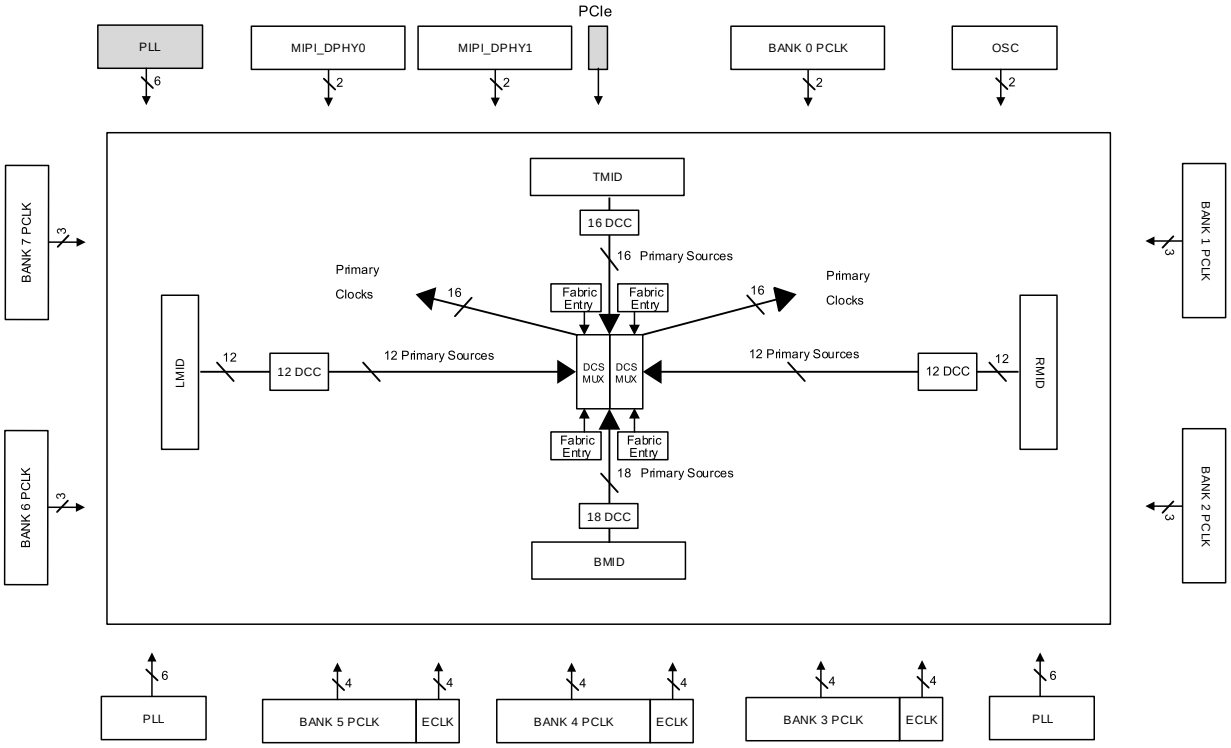


Figure 2.7. Clocking

2.3.4. Primary Clocks

The CrossLink-NX device family provides low-skew, high fan-out clock distribution to all synchronous elements in the FPGA fabric through the Primary Clock Network. The CrossLink-NX PCLK clock network is a balanced clock structure which is designed to minimize the clock skew among all the final destination of the IPs in the FPGA core that needs a clock source.

The primary clock network is divided into two clock domains depending on the device density. Each of these domains has 16 clocks that can be distributed to the fabric in the domain.

The Lattice Radiant software can automatically route each clock to one of the domains up to a maximum of 16 clocks per domain. You can change how the clocks are routed by specifying a preference in the Lattice Radiant software to locate the clock to a specific domain. The CrossLink-NX device provides you with a maximum of 64 unique clock input sources that can be routed to the primary Clock network.

Primary clock sources are:

- Dedicated clock input pins
- PLL outputs
- PCLKDIV, ECLKDIV outputs
- Internal FPGA fabric entries (with minimum general routing)
- SGMII-CDR, D-PHY, PCIe clocks
- OSC clock

These sources are routed to each of four clock switches called a Mid Mux (LMID, RMID, TMID, BMID). The outputs of the Mid MUX are routed to the center of the FPGA where additional clock switches (DSC_CMUX) are used to route the primary clock sources to primary clock distribution to the CrossLink-NX fabric. These routing muxs are shown in Figure 2.7. There are potentially 64 unique clock domains that can be used in the largest CrossLink-NX Device. For more information about the primary clock tree and connections, refer to CrossLink-NX sysCLOCK PLL/DLL Design and Usage Guide (FPGA-TN-02095).

2.3.5. Edge Clock

CrossLink-NX devices have a number of high-speed edge clocks that are intended for use with the PIO in the implementation of high-speed interfaces. There are four (4) ECLK networks per bank I/O on the Bottom side of the devices. For power management, the Edge clock network is powered by a separate power domain (to reduce power noise injection from the core and reduce overall noise induced jitter) while controlled by the same logic that gates the FPGA core and PCLK domains.

Each Edge Clock can be sourced from the following:

- Dedicated PIO Clock input pins (PCLK)
- DLLDEL output (PIO Clock delayed by 90°)
- PLL outputs (CLKOP, CLKOS, CLKOS2, CLKOS3, CLKOS4, and CLKOS5)
- Internal Nodes

Figure 2.8 illustrates the various ECLK sources. Bank 3 is shown in the example. Bank 4 and Bank 5 are similar.

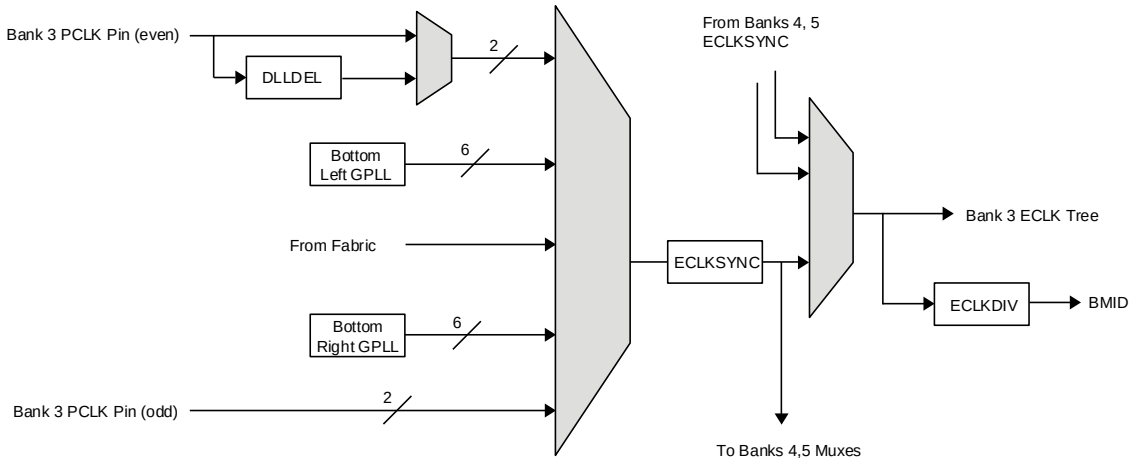


Figure 2.8. Edge Clock Sources per Bank

The edge clocks have low injection delay and low skew. They are typically used for DDR Memory or Generic DDR interfaces. For detailed information on Edge Clock connections, refer to CrossLink-NX sysCLOCK PLL/DLL Design and Usage Guide (FPGA-TN-02095).

2.3.6. Clock Dividers

CrossLink-NX devices have two distinct types of clock divider, Primary and Edge. There are from one (1) to eight (8) Primary Clock Divider (PCLKDIV) and which are located in the DCS_CMUX block(s) at the center of the device. There are twelve (12) ECLKDIV dividers per device, locate near the bottom high-speed I/O banks.

The PCLKDIV supports ÷2, ÷4, ÷8, ÷16, ÷32, ÷64, ÷128, and ÷1 (bypass) operation. The PCLKDIV is fed from a DCSMUX within the DCS_CMUX block. The clock divider output drives one input of the DCS Dynamic Clock Select within the DSC_CMUX block. The Reset (RST) control signal is asynchronously and forces all outputs to low. The divider output starts at next cycle after the reset is synchronously released. The PCLKDIV is shown in context in Figure 2.9.

The ECLKDIV is intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷3.5, ÷4, or ÷5 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The ECLKDIV can be fed from selected PLL outputs, external primary clock pins (with or without DLLDEL Delay) or from routing. The clock divider outputs feed into the Bottom Mid-mux (BMID). The Reset (RST) control signal is asynchronously and forces all outputs to low. The divider output starts at next cycle after the reset is synchronously released.

The ECLKDIV block is shown in context in Figure 2.8. For further information on clock dividers, refer to CrossLink-NX sysCLOCK PLL/DLL Design and Usage Guide (FPGA-TN-02095).

2.3.7. Clock Center Multiplexor Blocks

All clock sources are selected and combined for primary clock routing through the Dynamic Clock Selector Center Multiplexor logic (DCS_CMUX). There are one (1) or two (2) DCS_CMUX blocks per device. Each DCS_CMUX block contains 2 DCSMUX blocks, 1 PCLKDIV, 1 DCS block, and 1 or 2 CMUX blocks. See Figure 2.9 for a representative DCS_CMUX block diagram.

The heart of the DCS_CMUX is the Center Multiplexor (CMUX) block, inputs up to 64 feed clock sources (Mid-muxes (RMID, LMID, TMIC, BMID) and DCC) and to drive up to 16 primary clock trunk lines.

Up to two (2) clock inputs to the DCS_CMUX can be routed through a Dynamic Clock Select block then routed to the CMUX. One (1) input to the DCS can be optionally divided by the Primary Clock Divider (PCLKDIV). For more information about the DCS_CMUX, refer to CrossLink-NX sysCLOCK PLL/DLL Design and Usage Guide (FPGA-TN-02095).

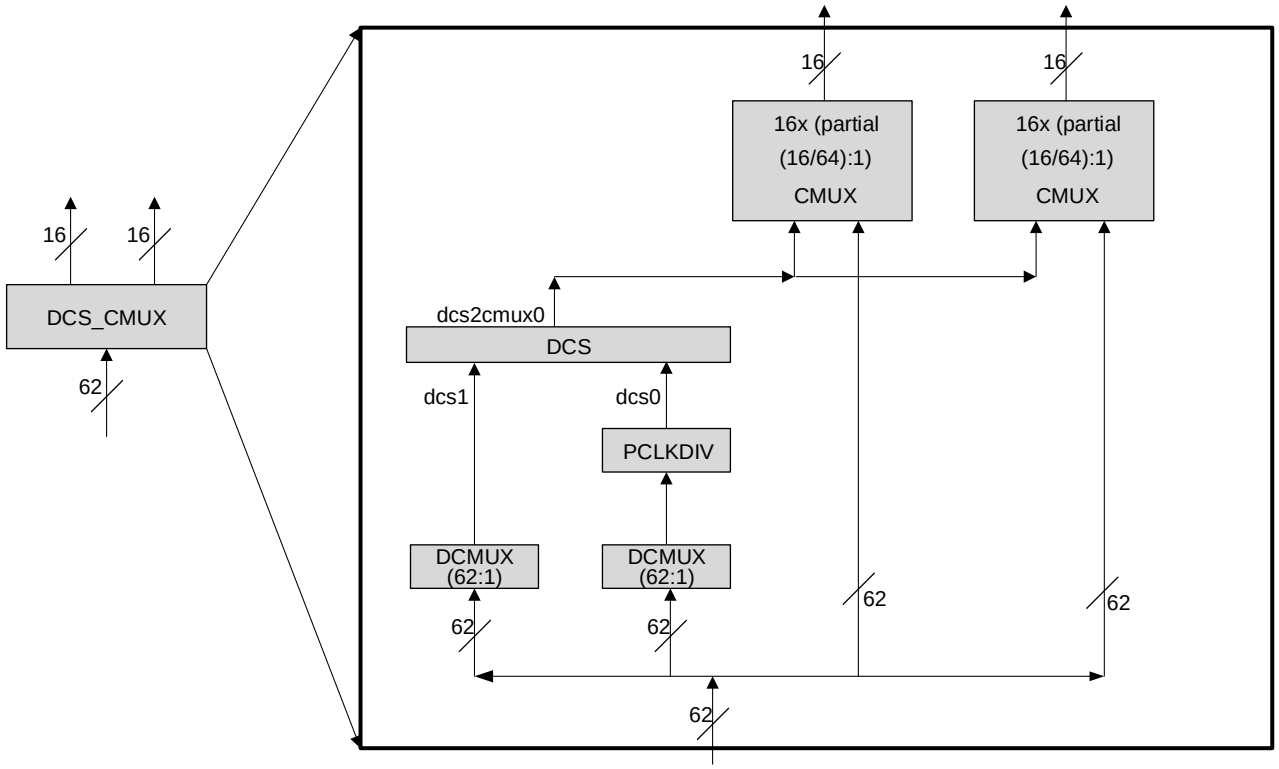


Figure 2.9. DCS_CMUX Diagram

2.3.8. Dynamic Clock Select

The Dynamic Clock Select (DCS) is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources. Depending on the operation modes, it switches between two (2) independent input clock sources either with or without any glitches. This is achieved regardless of when the select signal is toggled. Both input clocks must be running to achieve functioning glitchless DCS output clock, but running clocks are not required when used as non-glitchless normal clock multiplexer.

There are one (1) or two (2) DCS blocks per device that feed all clock domains. The DCS blocks are located in the DCS_MUX block. The inputs to the DCS blocks come from MIDMUX outputs and user logic clocks via DCC elements. The DCS elements are located at the center of the PLC array core. The output of the DCS is connected to the inputs of Primary Clock Center MUXs (CMUX).

Figure 2.10 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, refer to CrossLink-NX sysCLOCK PLL/DLL Design and Usage Guide (FPGA-TN-02095).

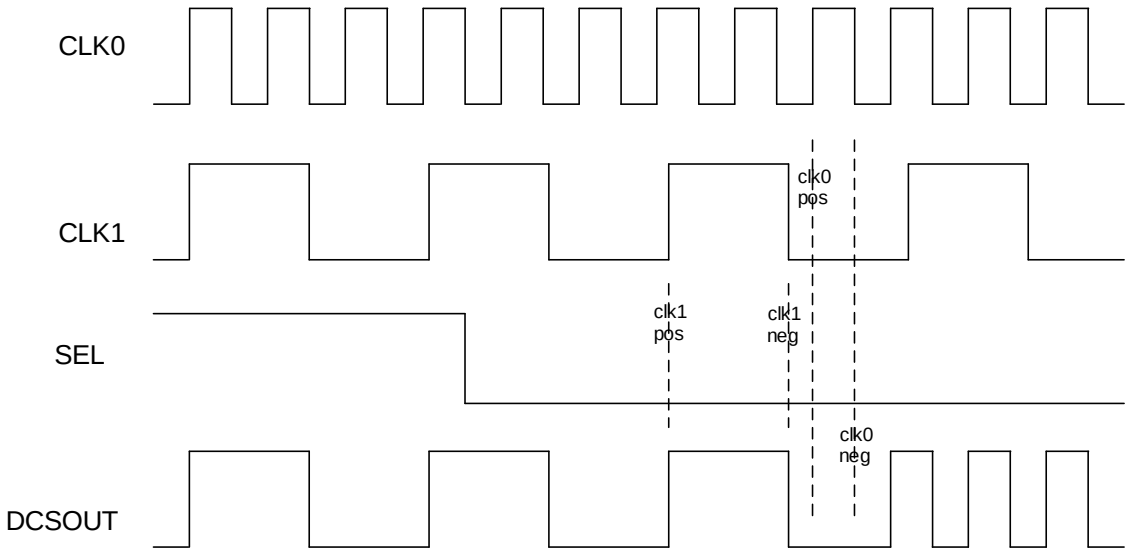


Figure 2.10. DCS Waveforms

2.3.9. Dynamic Clock Control

The Dynamic Clock Control (DCC), Domain Clock enable/disable feature allows internal logic control of the domain primary clock network. When a clock network is disabled, the clock signal is static and not toggle. All the logic fed by that clock does not toggle, reducing the overall power consumption of the device. The disable function is glitchless, and does not increase the clock latency to the primary clock network.

Four additional DCC elements control the clock inputs from the CrossLink-NX domain logic to the Center MUX elements (DSC_CMUX).

This DCC controls the clock sources from the Primary CLOCK MIDMUX before they are fed to the Primary Center MUXs that drive the domain clock network. For more information about the DCC, refer to CrossLink-NX sysCLOCK PLL/DLL Design and Usage Guide (FPGA-TN-02095).

2.3.10. DDRDLL

CrossLink-NX has 2 identical DDRDLL blocks, located in the lower left and lower right corners of the device. Each DDRDLL (master DLL block) can generate a phase shift code representing the amount of delay in a delay block that corresponding to 90-degree phase of the reference clock input, and provide this code to every individual DQS block and DLLDEL slave delay element. The reference clock can be either from PLL, or input pin. This code is used in the DQSBUF block that controls a set of DQS pin groups to interface with DDR memory (slave DLL). The DQSBUF uses this code to controls the DQS input of the DDR memory to 90 degree shift to clock DQs at the center of the data eye for DDR memory interface.

- The code is also sent to another slave DLL, DLLDEL, that takes a primary clock input and generates a 90 degree shift clock output to drive the clocking structure. This is useful to interface edge-aligned Generic DDR, where 90 degree clocking needs to be created. Not all primary clock inputs have associated DLLDEL control. Figure 2.11 shows DDRDLL connectivity to a DLLDEL block (connectivity to DQSBUF blocks is similar).

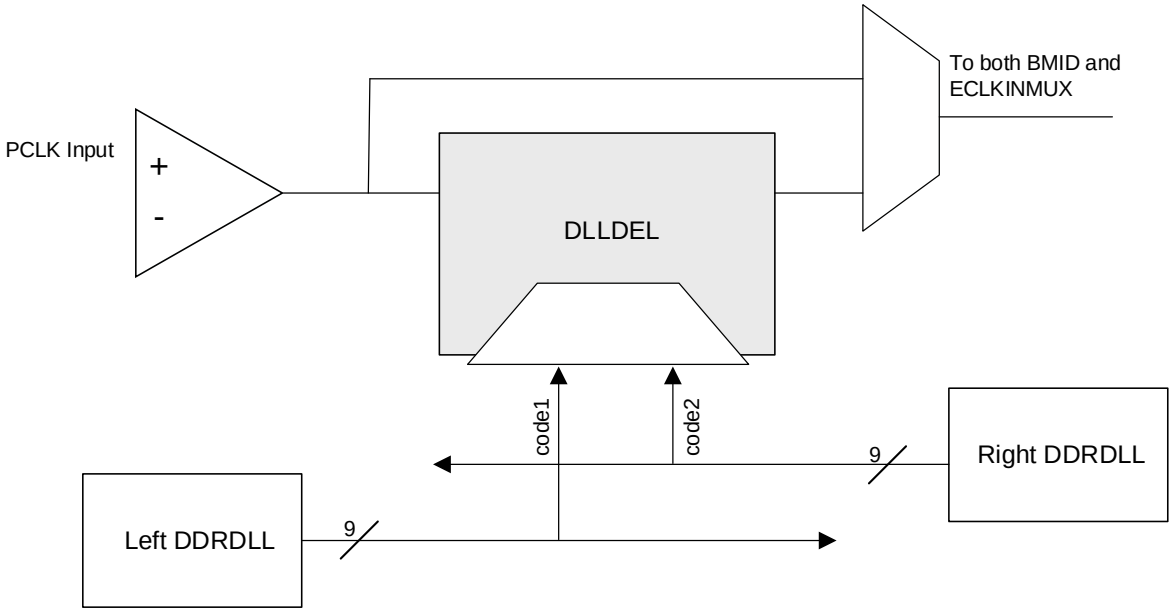


Figure 2.11. DLLDEL Functional Diagram

Each DDRDLL can generate delay code based on the reference clock frequency. The slave DLL (DQSBUF and DLLDEL) use the code to delay the signal, to create the phase shifted signal used for either DDR memory, or creating 90 degree shift clock. Figure 2.12 shows the DDRDLL and the slave DLLs on the top level view.

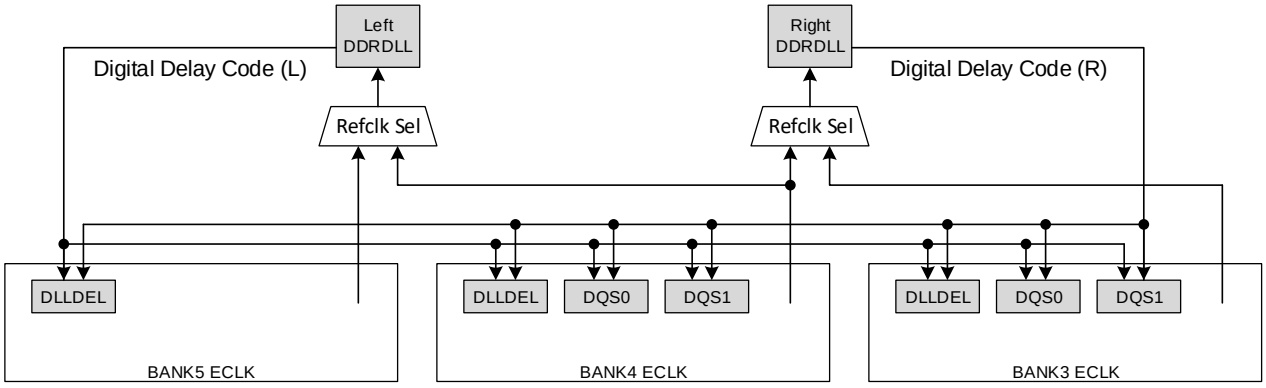


Figure 2.12. CrossLink-NX DDRDLL Architecture

2.4. SGMII Clock Data Recovery (CDR)

The CrossLink-NX-40 Device includes two hardened Clock Data Recovery (CDR). The CDR's enables Serial Gigabit Media Independent Interface (SGMII) solutions. There are three main blocks in each CDR, the CDR, deserializer and FIFO. Each CDR features two loops. The first loop is locked to the reference clock. Once locked, the loop switches to the data path loop where the CDR tracks the data signals to generate the correcting signals needed to achieve and maintain phase lock with the data. The data is then passed through a deserializer which deserialize the data to 10-bit parallel data. The 10-bit parallel data is then sent to the FIFO bridge which allows the CDR to interface with the rest of the FPGA.

Figure 2.13 shows a block diagram of the SGMII CDR IP.

The two hardened blocks are located at the bottom left of the chip and uses the high speed I/O Bank 5 for the differential pair input. It is recommended that the reference clock should be entered through a GPIO that has connection to the PLL on the lower left corner as well.

For more information about how to implement the hardened CDR for your SGMII solution, refer to the CrossLink-NX High-Speed I/O Interface (FPGA-TN-02097).

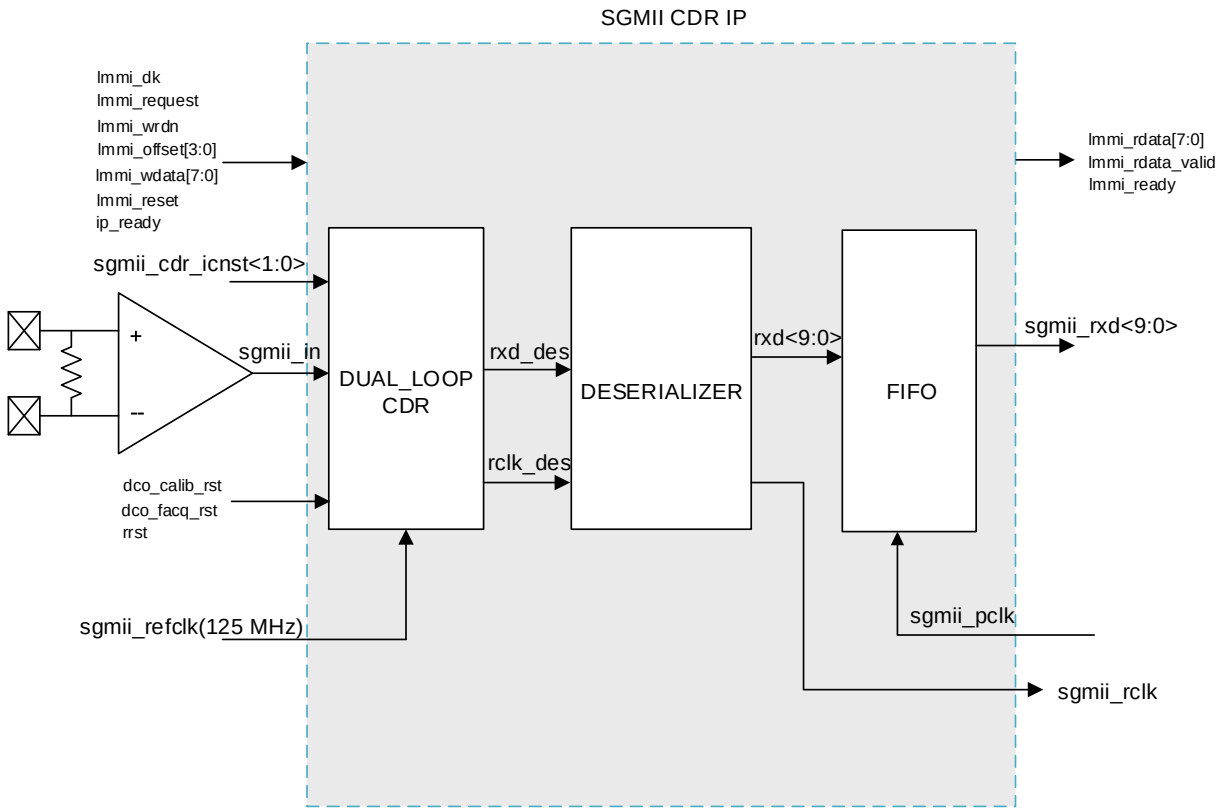


Figure 2.13. SGMII CDR IP

2.5. sysMEM Memory

CrossLink-NX devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18 Kb RAM with memory core, dedicated input registers and output registers as well as optional pipeline registers at the outputs. Each EBR includes functionality to support true dual-port, pseudo dual-port, single-port RAM, ROM and built in FIFO. In CrossLink-NX, unused EBR blocks is powered down to minimize power consumption.

2.5.1. sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as listed in Table 2.4. FIFO's can be implemented using the built in read and write address counters and programmable full, almost full, empty and almost empty flags. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with 18-bit and 36-bit data widths. For more information, refer to CrossLink-NX Memory Usage Guide (FPGA-TN-02094).

EBR also provides a build in ECC engine. The ECC engine supports a write data width of 32 bits and it can be cascaded for larger data widths such as x64. The ECC parity generator creates and stores parity data for each 32-bit word written. When a read operation is performed, it compares the data with its associated parity data and report back if any Single Event Upset (SEU) event has disturbed the data. Any single bit data disturb is automatically corrected at the data output. In addition, two dedicated error flags indicate if a single-bit or two-bit error has occurred.

Table 2.4. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1
	8,192 x 2
	4,096 x 4
	2,048 x 9
	1,024 x 18
	512 x 36
True Dual Port	16,384 x 1
	8,192 x 2
	4,096 x 4
	2,048 x 9
	1,024 x 18
Pseudo Dual Port	16,384 x 1
	8,192 x 2
	4,096 x 4
	2,048 x 9
	1,024 x 18
	512 x 36

2.5.2. Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports (except ECC mode which only supports a write data width of 32 bits). The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

2.5.3. RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

2.5.4. Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

2.5.5. Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes, the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

2.5.6. Memory Output Reset

The EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2.14. The optional Pipeline Registers at the outputs of both ports are also reset in the same way.

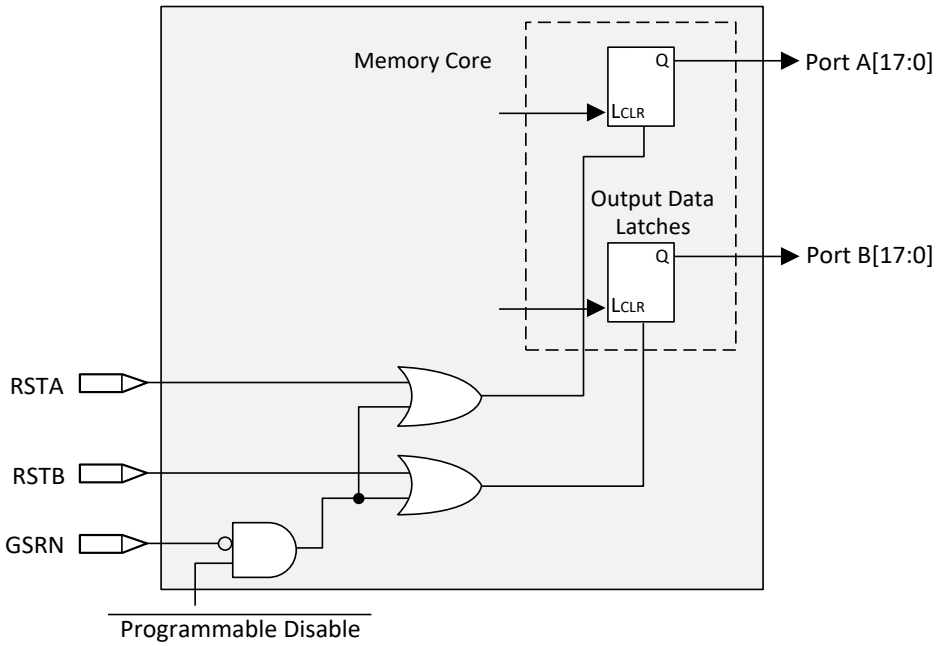


Figure 2.14. Memory Core Reset

For further information on the sysMEM EBR block, see the list of technical documentation in Supplemental Information section.

2.6. Large RAM

The CrossLink-NX device includes additional memory resources in the form of Large Random-Access Memory (LRAM) blocks.

The LRAM is designed to work as Single-Port RAM, Dual-Port RAM, Pseudo Dual-Port RAM, and ROM memories. It is meant to function as additional memory resources for you beyond what is available in the EBR and PFU.

Each individual Large RAM block contains 0.5 Mbit of memory, and has a programmable data width of up to 32 bits. Cascading Large RAM blocks allows data widths of up to 64 bits. Additionally, there is the ability to use either Error Correction Coding (ECC) or byte enable.

2.7. sysDSP

The CrossLink-NX family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

2.7.1. sysDSP Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. In the CrossLink-NX device family, there are many DSP blocks that can be used to support different data widths. This allows you to use highly parallel implementations of DSP functions. You can optimize DSP performance versus area by choosing appropriate levels of parallelism. Figure 2.15 compares the fully serial implementation to the mixed parallel and serial implementation.

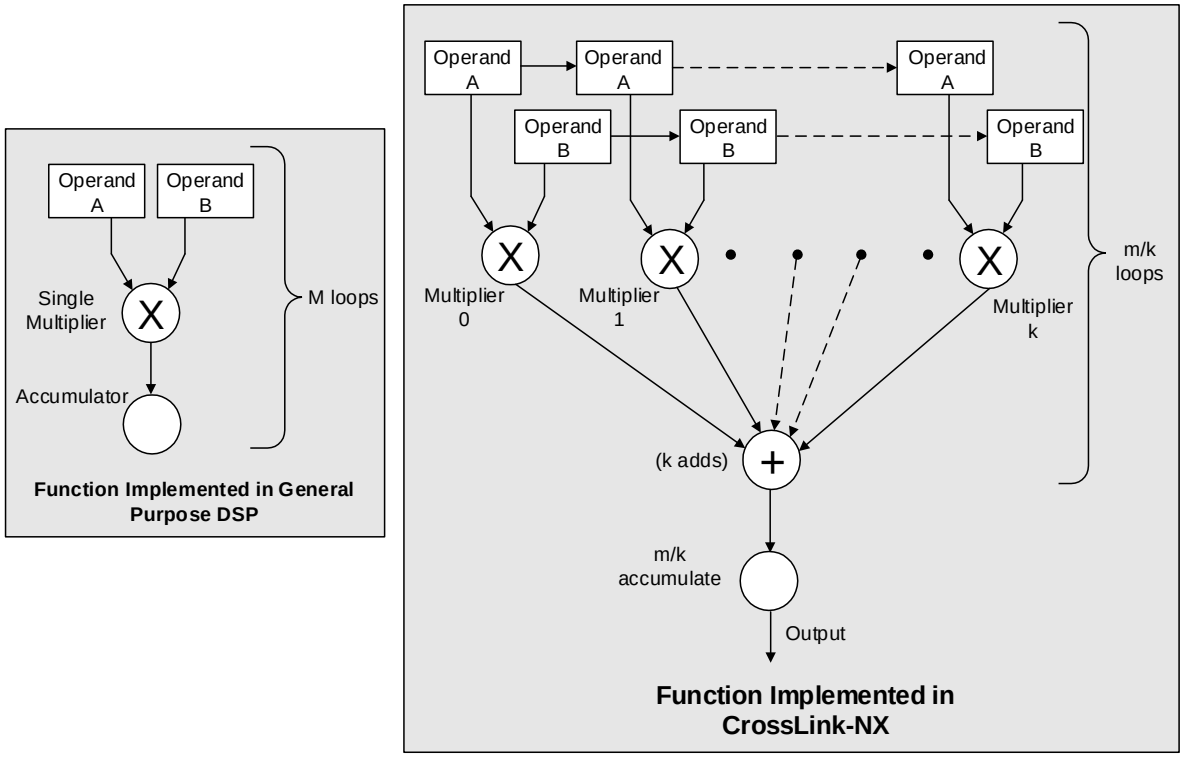


Figure 2.15. Comparison of General DSP and CrossLink-NX Approaches

2.7.2. sysDSP Architecture Features

The CrossLink-NX sysDSP Slice has been significantly enhanced to provide functions needed for advanced processing applications. These enhancements provide improved flexibility and resource utilization.

The CrossLink-NX sysDSP Slice supports many functions that include the following:

- Symmetry support. The primary target application is wireless. 1D Symmetry is useful for many applications that use FIR filters when their coefficients have symmetry or asymmetry characteristics. The main motivation for using 1D symmetry is cost/size optimization. The expected size reduction is up to 2x.
  - Odd Mode – Filter with Odd number of taps
  - Even Mode – Filter with Even number of taps
  - Two dimensional (2D) Symmetry Mode – Supports 2D filters for mainly video applications
- Dual-multiplier architecture. Lower accumulator overhead to half and the latency to half compared to single multiplier architecture.
- Fully cascadable DSP across slices. Support for symmetric, asymmetric and non-symmetric filters.
- Multiply (36 x 36, two 18 x 36, four 18 x 18 or eight 9 x 9)
- Multiply Accumulate (supports one 18 x 36 multiplier result accumulation, two 18 x 18 multiplier result accumulation or four 9 x 9 multiplier result accumulation)
- Two Multiplies feeding one Accumulate per cycle for increased processing with lower latency (two 18 x 18 Multiplies feed into an accumulator that can accumulate up to 54 bits)
- Pipeline registers
- 1D Symmetry support. The coefficients of FIR filters have symmetry or negative symmetry characteristics.
  - Odd Mode – Filter with Odd number of taps
  - Even Mode – Filter with Even number of taps
- 2D Symmetry support. The coefficients of 2D FIR filters have symmetry or negative symmetry characteristics.
  - 3*3 and 3*5 – Internal DSP Slice support
  - 5*5 and larger size 2D blocks – Semi internal DSP Slice support

- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading DSP blocks
  - Minimizes fabric use for common DSP functions
  - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
  - Provides matching pipeline registers
  - Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- RTL Synthesis friendly synchronous reset on all registers, while still supporting asynchronous reset for legacy users
- Dynamic MUX selection to allow Time Division Multiplexing (TDM) of resources for applications that require processor-like flexibility that enables different functions for each clock cycle

For most cases, as shown in Figure 2.16, the CrossLink-NX sysDSP is backwards-compatible with the LatticeECP3™ sysDSP block, such that, legacy applications can be targeted to CrossLink-NX sysDSP. Figure 2.16 shows the diagram of sysDSP.

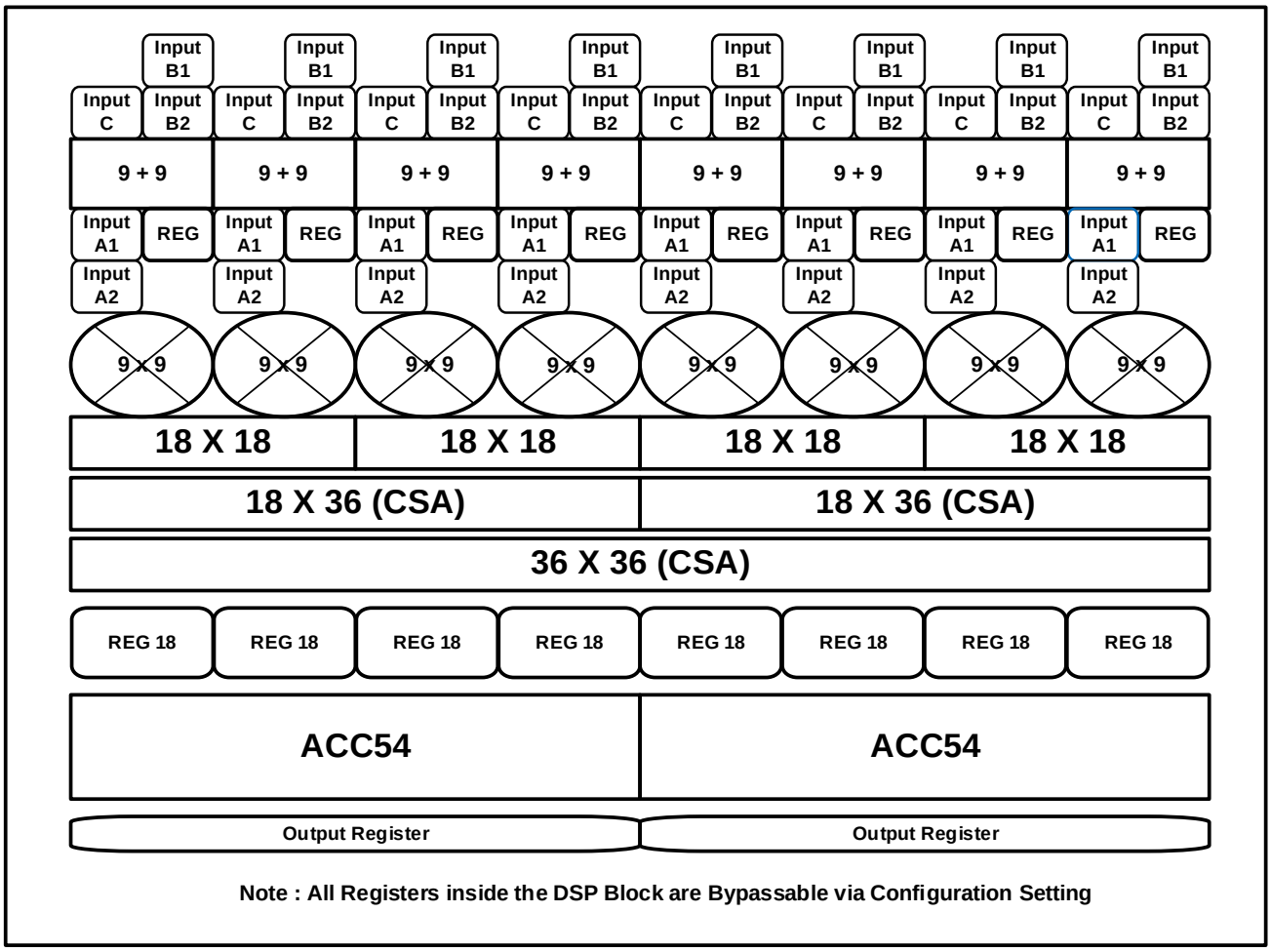


Figure 2.16. CrossLink-NX DSP Functional Block Diagram

The CrossLink-NX sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2.5 shows the capabilities of CrossLink-NX sysDSP block versus the above functions.

Table 2.5. Maximum Number of Elements in a sysDSP block

Width of Multiply	x9	x18	x36
MULT	8	4	1
MAC	2	2	—
MULTADDSUB	2	2	—
MULTADDSUBSUM	2	2	—

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting *dynamic operation,* the following operations are possible:

- In the Add/Sub option, the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

For further information, refer to CrossLink-NX sysDSP Usage Guide (FPGA-TN-02096).

2.8. Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysI/O buffers and pads. On the CrossLink-NX devices, the Programmable I/O cells (PIC) are assembled into groups of two PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the CrossLink-NX devices, two adjacent PIO can be combined to provide a complementary output driver pair.

2.9. Programmable I/O Cell (PIC)

CrossLink-NX is consists of base PIC and gearing PIC. Base PIC covers the top, left, and right bank while the gearing PIC covers only the bottom banks that supports DDR operation. Gearing PIC contains the edge monitor for optimizing delay setting to locate the center of data window.

The PIC contains three blocks: an input register block, output register block, and tristate register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

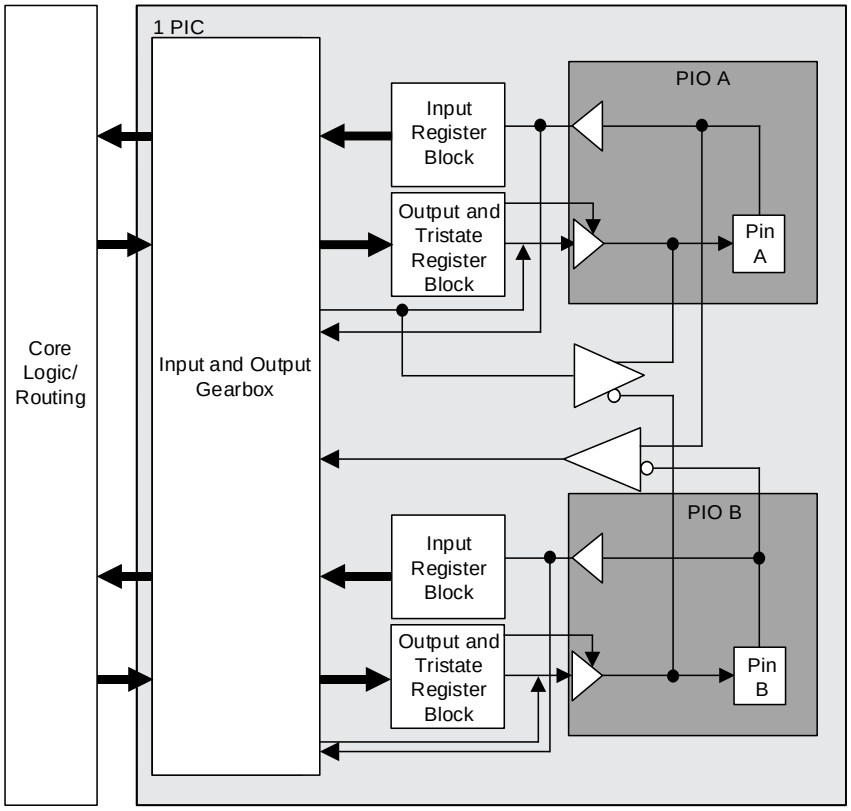


Figure 2.17. Group of Two High Performance Programmable I/O Cells

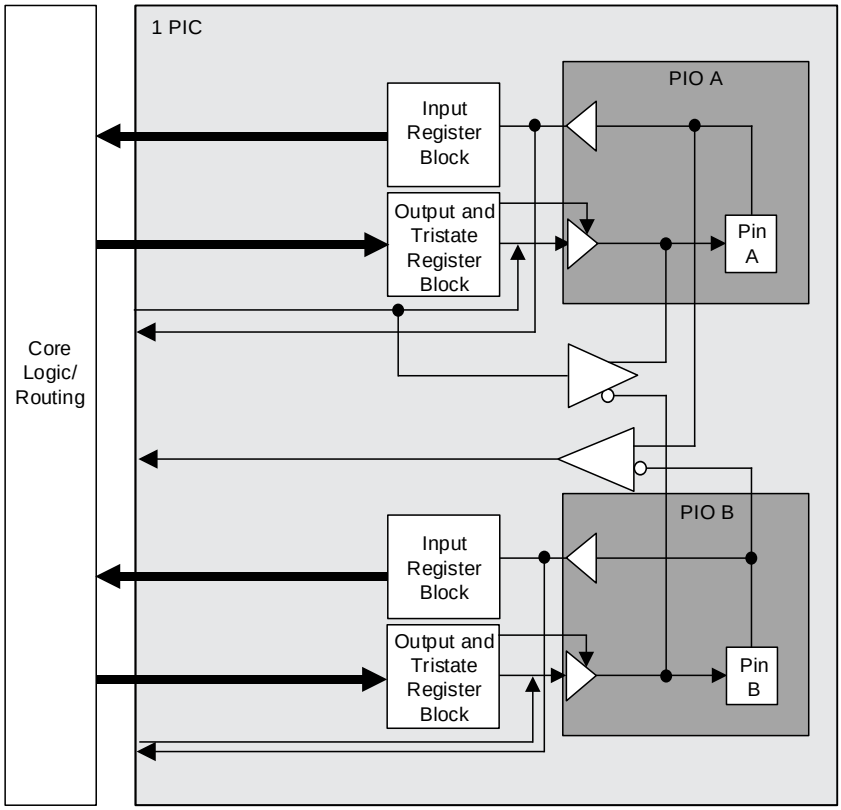


Figure 2.18. Wide Range Programmable I/O Cells

2.9.1. Input Register Block

The input register blocks for the PIO on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core. In addition, the input register blocks for the PIO on the bottom edges include built-in FIFO logic to interface to DDR and LPDDR memory.

The Input register block on the bottom side includes gearing logic and registers to implement IDDRX1, IDDRX2, IDDRX4, IDDRX5 gearing functions. With two PICs sharing the DDR register path, it can also implement IDDRX71 function used for 7:1 LVDS interfaces. It uses three sets of registers – shift, update, and transfer to implement gearing and the clock domain transfer. The first stage registers samples the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. For more information on gearing function, refer to CrossLink-NX High-Speed I/O Interface (FPGA-TN-02097).

2.9.2.1. Input FIFO

The CrossLink-NX PIO has dedicated input FIFO per single-ended pin for input data register for DDR Memory interfaces. The FIFO resides before the gearing logic. It transfers data from DQS domain to continuous ECLK domain. On the Write side of the FIFO, it is clocked by DQS clock, which is the delayed version of the DQS Strobe signal from DDR memory. On the Read side of FIFO, it is clocked by ECLK. ECLK may be any high-speed clock with identical frequency as DQS (the frequency of the memory chip). Each DQS group has one FIFO control block. It distributes FIFO read/write pointer to every PIC in same DQS group. DQS Grouping and DQS Control Block is described in DDR Memory Support section.

Table 2.6. Input Block Port Description

Name	Type	Description
D	Input	High Speed Data Input
Q[1:0]/Q[3:0]/Q[6:0]/Q[7:0]/Q[9:0]	Output	Low Speed Data to the device core
RST	Input	Reset to the Output Block
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQS	Input	Clock from DQS control Block used to clock DDR memory data
ALIGNWD	Input	Data Alignment signal from device core.

Figure 2.19 shows the input register block for the PIO on the top, left, and right edges.

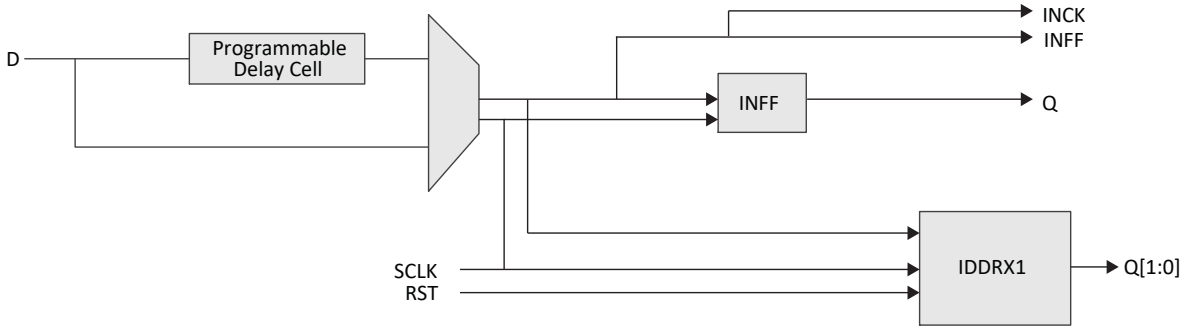
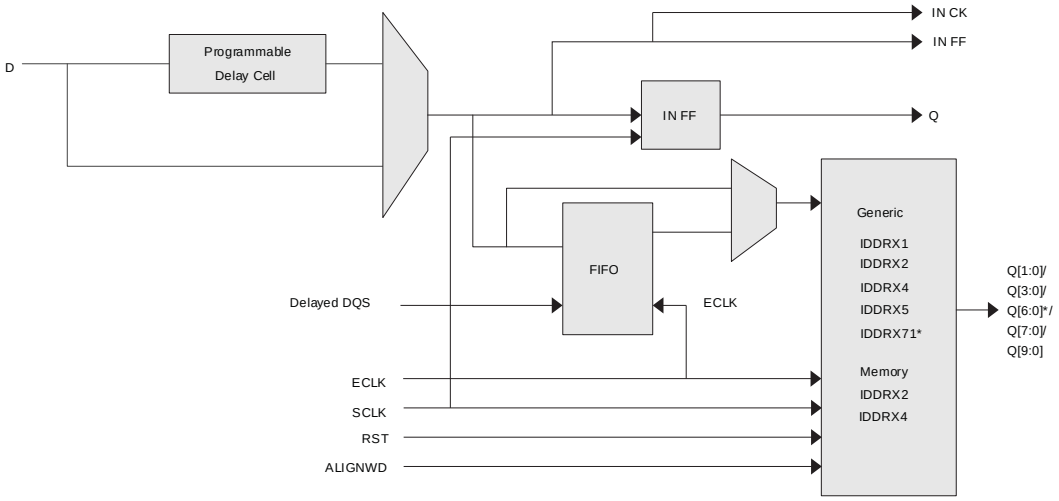


Figure 2.19. Input Register Block for PIO on Top, Left, and Right Sides of the Device

Figure 2.20 shows the input register block for the PIO located on the bottom edge.



*For 7:1 LVDS interface only. It is required to use PIO pair pins (PIOA/B or PIOC/D).

Figure 2.20. Input Register Block for PIO on Bottom Side of the Device

2.9.2. Output Register Block

The output register block registers signal from the core of the device before they are passed to the sysI/O buffers.

CrossLink-NX output data path has output programmable flip flops and output gearing logic. On the bottom side, the output register block can support 1x, 2x, x4, x5, and 7:1 gearing enabling high speed DDR interfaces and DDR memory interfaces. On the top, left, and right sides, the banks support 1x gearing. CrossLink-NX output data path diagram is shown in Figure 2.21. The programmable delay cells are also available in the output data path.

For detailed description of the output register block modes and usage, you can refer to CrossLink-NX High-Speed I/O Interface (FPGA-TN-02097).

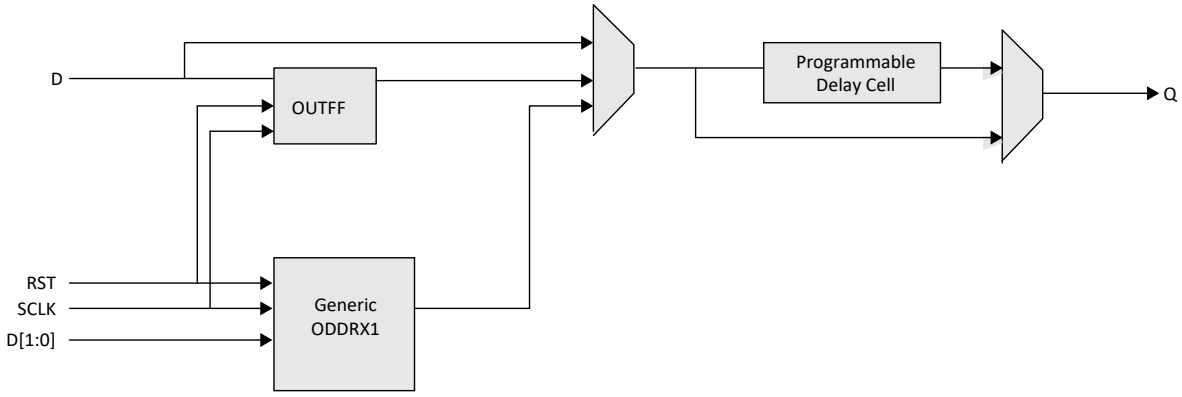
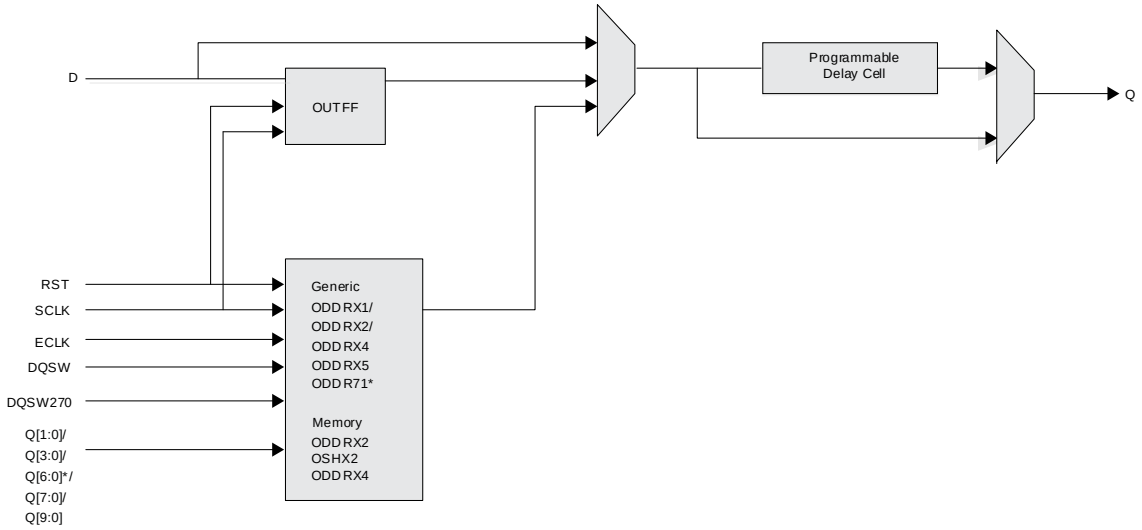


Figure 2.21. Output Register Block on Top, Left, and Right Sides



*For 7:1 LVDS interface only. It is required to use PIO pair pins PIOA/B.

Figure 2.22. Output Register Block on Bottom Side

Table 2.7. Output Block Port Description

Name	Type	Description
Q	Output	High Speed Data Output
D	Input	Data from core to output SDR register
Q[1:0]/Q[3:0]/Q[6:0]/Q[7:0]/Q[9:0]	Input	Low Speed Data from device core to output DDR register
RST	Input	Reset to the Output Block
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQSW	Input	Clock from DQS control Block used to generate DDR memory DQS output
DQSW270	Input	Clock from DQS control Block used to generate DDR memory DQ output

2.10. Tristate Register Block

The tristate register block registers tristate control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output. In DDR, operation used mainly for DDR memory interface can be implemented on the bottom side of the device. Here, two inputs feed the tristate registers clocked by both ECLK and SCLK.

Figure 2.23 and Figure 2.24 show the Tristate Register Block functions on the device. For detailed description of the tristate register block modes and usage, you can refer to CrossLink-NX High-Speed I/O Interface (FPGA-TN-02097).

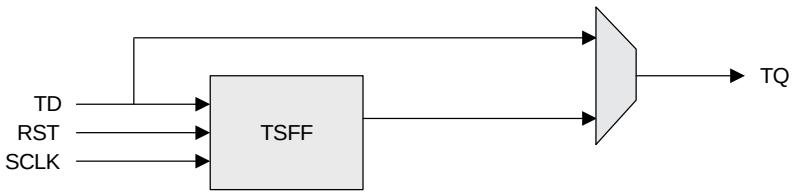


Figure 2.23. Tristate Register Block on Top, Left, and Right Sides

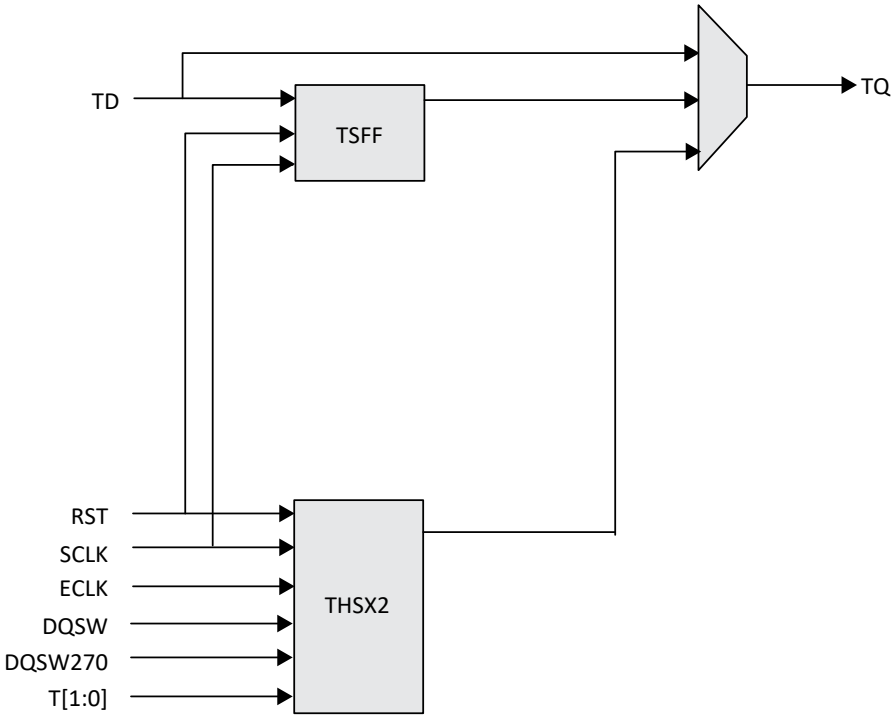


Figure 2.24. Tristate Register Block on Bottom Side

Table 2.8. Tristate Block Port Description

Name	Type	Description
TD	Input	Tristate Input to Tristate SDR Register
RST	Input	Reset to the Tristate Block
TD[1:0]	Input	Tristate input to TSHX2 function
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQSW	Input	Clock from DQS control Block used to generate DDR memory DQS output
DQSW270	Input	Clock from DQS control Block used to generate DDR memory DQ output
TQ	Output	Output of the Tristate block

2.11. DDR Memory Support

2.11.1. DQS Grouping for DDR Memory

Certain PICs have additional circuitry to allow the implementation of high-speed source synchronous and DDR3/DDR3L, LPDDR2 or LPDDR3 memory interfaces. The support varies by the edge of the device as detailed below.

The Bottom bank PIC have fully functional elements supporting DDR3/DDR3L, LPDDR2, or LPDDR3 memory interfaces. Every 16 PIO on the bottom side are grouped into one DQS group, as shown in Figure 2.25. Within each DQS group, there are two pre-placed pins for DQS and DQS# signals. The rest of the pins in the DQS group can be used as DQ signals and DM signal. The number of pins in each DQS group bonded out is package dependent. DQS groups with less than 11 pins bonded out can only be used for LPDDR2/3 Command/ Address busses. In DQS groups with more than 11 pins bonded out, up to two pre-defined pins are assigned to be used as virtual VCCIO, by driving these pins to HIGH, and connecting these pins to VCCIO power supply. These connections create soft connections to VCCIO thru these output pins, and make better connections on VCCIO to help to reduce SSO noise. For details, refer to CrossLink-NX High-Speed I/O Interface (FPGA-TN-02097).

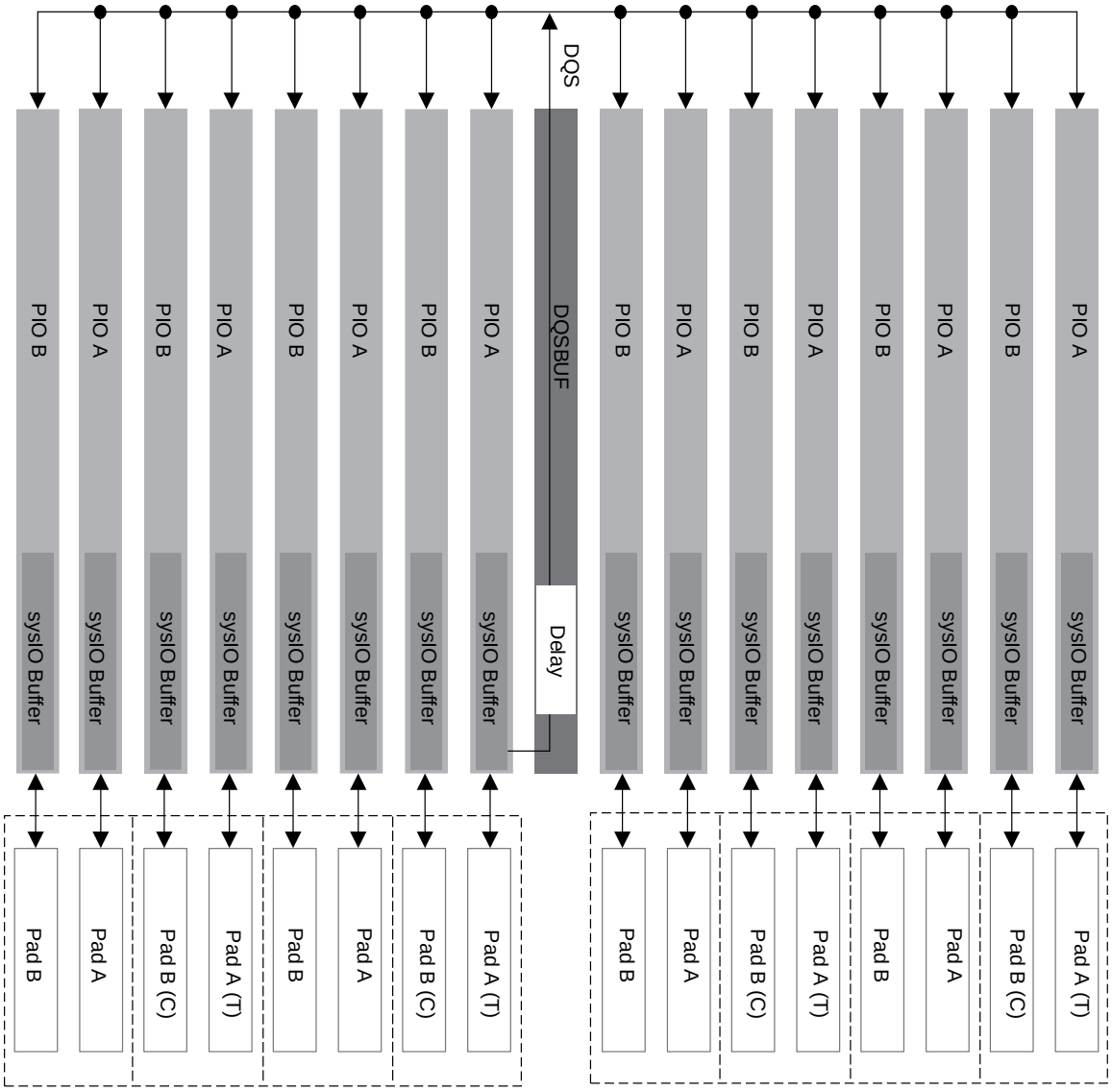


Figure 2.25. DQS Grouping on the Bottom Edge

2.11.2. DLL Calibrated DQS Delay and Control Block (DQSBUF)

To support DDR memory interfaces (DDR3/DDR3L, LPDDR2/3), the DQS strobe signal from the memory must be used to capture the data (DQ) in the PIC registers during memory reads. This signal is output from the DDR memory device aligned to data transitions and must be time shifted before it can be used to capture data in the PIC. This time shifted is achieved by using DQSBUF programmable delay line in the DQS Delay Block (DQS read circuit). The DQSBUF is implemented as a slave delay line and works in conjunction with a master DDRDLL.

This block also includes slave delay line to generate delayed clocks used in the write side to generate DQ and DQS with correct phases within one DQS group. There is a third delay line inside this block used to provide write leveling feature for DDR write if needed.

Each of the read and write side delays can be dynamically shifted using margin control signals that can be controlled by the core logic.

FIFO Control Block include here generates the Read and Write Pointers for the FIFO block inside the Input Register Block. These pointers are generated to control the DQS to ECLK domain crossing using the FIFO module.

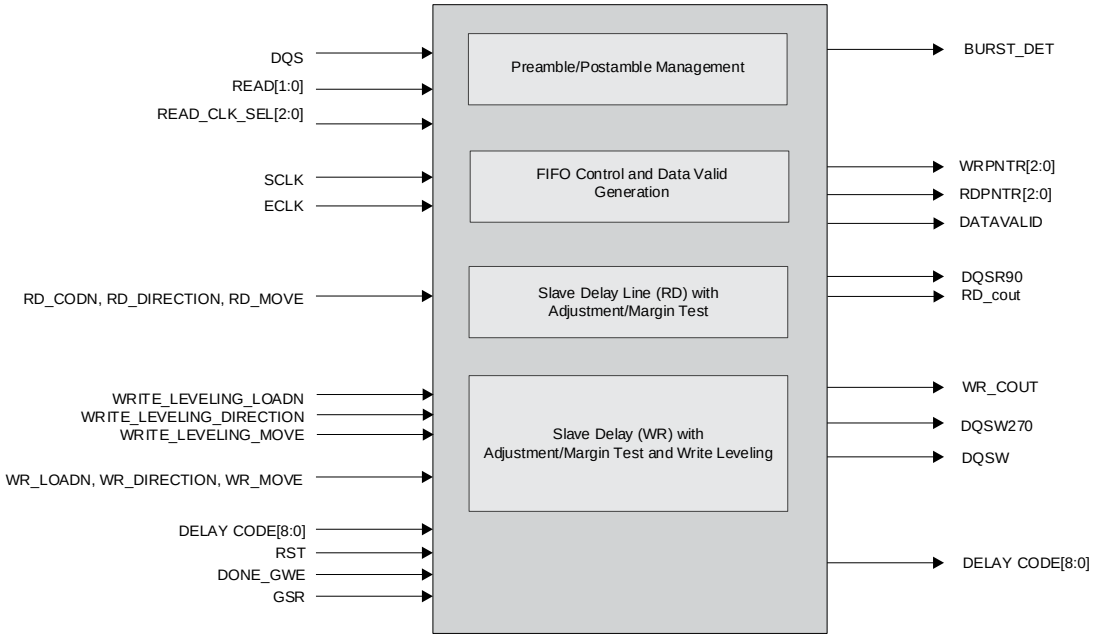


Figure 2.26. DQS Control and Delay Block (DQSBUF)

Table 2.9. DQSBUF Port List Description

Name	Type	Description
DQS	Input	DDR memory DQS strobe
READ[1:0]	Input	Read Input from DDR Controller
READCLKSEL[2:0]	Input	Read pulse selection
SCLK	Input	Slow System Clock
ECLK	Input	High Speed Edge Clock (same frequency as DDR memory)
RDLOADN, RDMOVE, RDDIRECTION	Input	Dynamic Margin Control ports for Read delay
WRLOADN, WRMOVE, WRDIRECTION	Input	Dynamic Margin Control ports for Write delay
DELAYCODE_I[8:0]	Input	Dynamic Delay Control
WRITE_LEVELING_LOADN, WRITE_LEVELING_DIRECTION, WRITE_LEVELING_MOVE	Input	Write Leveling Control
DQSR90	Output	90 delay DQS used for Read
DQSW270	Output	90 delay clock used for DQ Write
DQSW	Output	Clock used for DQS Write
RDPNTR[2:0]	Output	Read Pointer for IFIFO module
WRPNTR[2:0]	Output	Write Pointer for IFIFO module
DATAVALID	Output	Signal indicating start of valid data
BURSTDET	Output	Burst Detect indicator
RD_COUT	Output	Read Count
WR_COUT	Output	Write Count
DELAYCODE_O[8:0]	Output	Dynamic Delay Control

2.12. sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allows you to implement the wide variety of standards that are found in today's systems including LVDS, HSUL, SSTL Class I and II, LVCMOS, LVTTL, and MIPI.

The CrossLink-NX family contains multiple Programmable I/O Cell (PIC) blocks. Each PIC contains two Programmable I/O, PIOA and PIOB. Each PIO includes a sysI/O buffer and I/O logic. Two adjacent PIO can be joined to provide a differential I/O pair. These two pairs are referred to as True and Comp, where True Pad is associated with the positive side of the differential I/O, and the complement with the negative.

The top, left and right side banks support I/O standards from 3.3 V to 1.0 V while the bottom supports I/O standards from 1.8 V to 1.0 V. Every pair of I/O on the bottom bank also have a true LVDS and SLVS Tx Driver. In addition, the bottom bank supports single-ended input termination. Both static and dynamic termination are supported. Dynamic termination is used to support the DDR/LPDDR interface standards. For more information about DDR implementation in I/O Logic and DDR memory interface support, refer to CrossLink-NX High-Speed I/O Interface (FPGA-TN-02097).

2.12.1. Supported sysI/O Standards

CrossLink-NX sysI/O buffer supports both single-ended differential and differential standards. Single-ended standards can be further subdivided into internally ratioed standards such as LVCMOS, LVTTL, and externally referenced standards such as HSUL and SSTL. The buffers support the LVTTL, LVCMOS 1.0 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V standards. Differential standards supported include LVDS, SLVS, differential LVCMOS, differential SSTL, and differential HSUL. For better support of video standards, subLVDS and MIPI_D-PHY are also supported. Table 2.10 and Table 2.11 provide a list of sysI/O standards supported in CrossLink-NX devices.

Table 2.10. Single-Ended I/O Standards

Standard	Input	Output	Bi-directional
LVTTL33	Yes	Yes	Yes
LVCMOS33	Yes	Yes	Yes
LVCMOS25	Yes	Yes	Yes
LVCMOS18	Yes	Yes	Yes
LVCMOS15	Yes	Yes	Yes
LVCMOS12	Yes	Yes	Yes
LVCMOS10	Yes	No	No
HTSL15 I	Yes	Yes	Yes
SSTL 15 I	Yes	Yes	Yes
SSTL 135 I	Yes	Yes	Yes
HSUL12	Yes	Yes	Yes
LVCMOS18H	Yes	Yes	Yes
LVCMOS15H	Yes	Yes	Yes
LVCMOS12H	Yes	Yes	Yes
LVCMOS10H	Yes	Yes	Yes
LVCMOS10R	Yes	—	Yes*

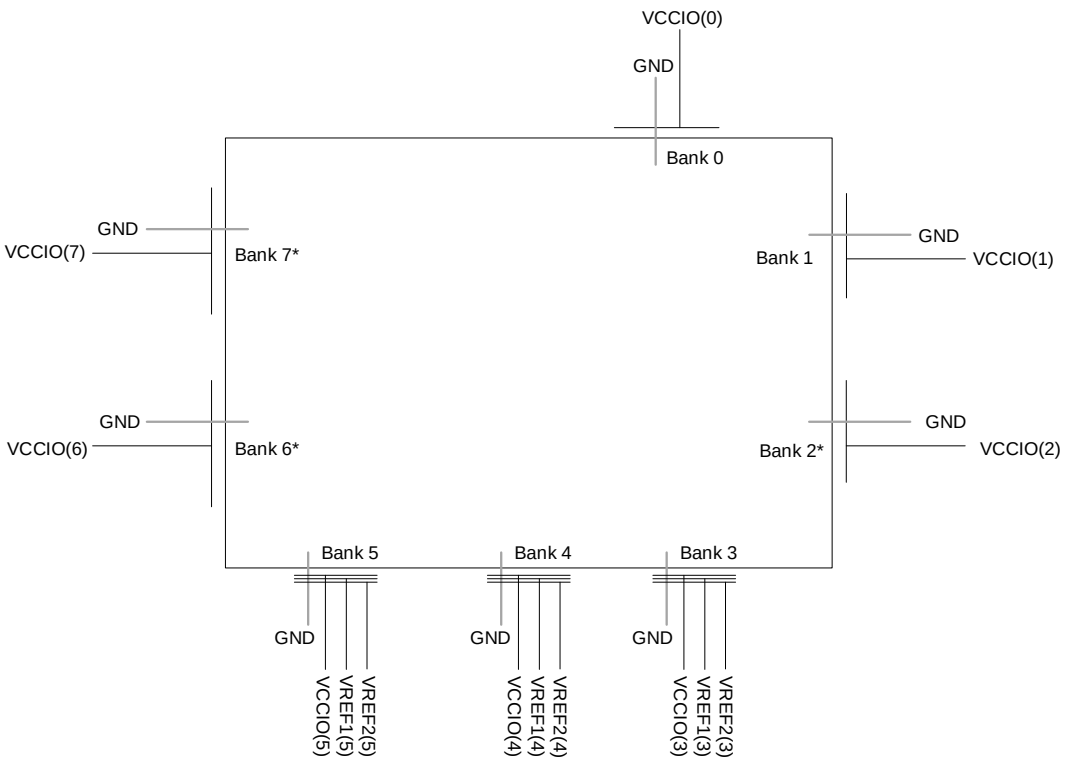
*Note: Output supported by LVCMOS10H.

Table 2.11. Differential I/O Standards

Standard	Input	Output	Bi-directional
LVDS	Yes	Yes	Yes
SUBLVDS	Yes	No	—
SLVS	Yes	Yes	—
SUBLVDSE	—	Yes	—
SUBLVDSEH	—	Yes	—
LVDSE	—	Yes	—
MIPI_D-PHY	Yes	Yes	Yes
HSTL15D_I	Yes	Yes	Yes
SSTL15D_I	Yes	Yes	Yes
SSTL15D_II	Yes	Yes	Yes
SSTL135D_I	Yes	Yes	Yes
SSTL135D_II	Yes	Yes	Yes
HSUL12D	Yes	Yes	Yes
LVTTL33D	—	Yes	—
LVCMOS33D	—	Yes	—
LVCMOS25D	—	Yes	—

2.12.2. sysI/O Banking Scheme

CrossLink-NX devices have up to eight banks in total. For 40K device, there are one bank on top, two banks each at left and right side of device, and three on the bottom side of device. For 17K device, one bank on top, one on right side and three on the bottom side of device. The higher density CrossLink-NX device has more pins in each bank. Bank 0, Bank 1, Bank 2, Bank 6, and Bank 7 support up to VCCIO 3.3 V while Bank 3, Bank 4, and Bank 5 support up to VCCIO 1.8 V. In addition, Bank 3, Bank 4, and Bank 5 support two VREF inputs for flexibility to receive two different referenced input levels on the same bank. Figure 2.27 shows the location of each bank.



***Note:** Bank not available in LIFCL-17.

Figure 2.27. sysI/O Banking

2.12.2.1. Typical sysI/O I/O Behavior During Power-up

The internal Power-On-Reset (POR) signal is deactivated when V_{CC} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is your responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in CrossLink-NX devices, see the list of technical documentation in Supplemental Information section.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify the system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. For different power supply voltage level by the I/O banks, please refer to CrossLink-NX sysI/O Usage Guide (FPGA-TN-02067) for detailed information.

2.12.2.2. VREF1 and VREF2

Bank 3, Bank 4, and Bank 5 can support two separate VREF input voltage, VREF1, and VREF2. To assign a VREF driver, use IO_Type = VREF1_DRIVER or VREF2_DRIVER. To assign VREF to a buffer, use VREF1_LOAD or VREF2_LOAD.

2.12.2.3. SysI/O Standards Supported by I/O Bank

All banks can support multiple I/O standards under the VCCIO rules discussed above. Table 2.12 and Table 2.13 summarize the I/O standards supported on various sides of the CrossLink-NX device.

Table 2.12. Single-Ended I/O Standards Supported on Various Sides

Standard	Top	Left*	Right	Bottom
LVTTL33	Yes	Yes	Yes	—
LVCMOS33	Yes	Yes	Yes	—
LVCMOS25	Yes	Yes	Yes	—
LVCMOS18	Yes	Yes	Yes	—
LVCMOS15	Yes	Yes	Yes	—
LVCMOS12	Yes	Yes	Yes	—
LVCMOS10	Yes	Yes	Yes	—
LVCMOS18H	—	—	—	Yes
LVCMOS15H	—	—	—	Yes
LVCMOS12H	—	—	—	Yes
LVCMOS10H	—	—	—	Yes
LVCMOS10R	—	—	—	Yes
HTSL15 I	—	—	—	Yes
SSTL 15 I, II	—	—	—	Yes
SSTL 135 I, II	—	—	—	Yes
HSUL12	—	—	—	Yes

*__Note:__ Left bank is not available in LIFCL-17.

Table 2.13. Differential I/O Standards Supported on Various Sides

Standard	Top	Left*	Right	Bottom
LVDS	—	—	—	Yes
SUBLVDS	—	—	—	Yes
SLVS	—	—	—	Yes
SUBLVDSE	Yes	Yes	Yes	—
SUBLVDSEH	—	—	—	Yes
LVDSE	Yes	Yes	Yes	—
MIPI_D-PHY	—	—	—	Yes
HSTL15D_I	—	—	—	Yes
SSTL15D_I	—	—	—	Yes
SSTL15D_II	—	—	—	Yes
SSTL135D_I	—	—	—	Yes
SSTL135D_II	—	—	—	Yes
HSUL12D	—	—	—	Yes
LVTTL33D	Yes	Yes	Yes	—
LVCMOS33D	Yes	Yes	Yes	—
LVCMOS25D	Yes	Yes	Yes	—

*__Note:__ Left bank is not available in LIFCL-17.

2.12.2.4. Hot Socketing

CrossLink-NX devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/O remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. Bank 0, Bank 1, Bank 2, Bank 6, and Bank 7 wide range I/O (excluding MCLK/MCSN/MOSI/INITN/DONE) are fully hot socket able while Bank 3, Bank 4, and Bank 5 are not supported.

2.12.3. sysI/O Buffer Configurations

This section describes the various sysI/O features available on the CrossLink-NX device. Refer to CrossLink-NX sysI/O Usage Guide (FPGA-TN-02067) for detailed information.

2.13. Analog Interface

The CrossLink-NX family provides an analog interface, consisting of two Analog to Digital Convertors (ADC), three continuous time comparators and an internal junction temperature monitoring diode. The two ADCs can sample the input sequentially or simultaneously.

2.13.1. Analog to Digital Converters

The Analog to Digital Convertor is a 12-bit, 1 MSPS SAR (Successive Approximation Resistor/capacitor) architecture converter. The ADC supports both continuous and single shot conversion modes.

The ADC input is selected among pre-selected GPIO input pairs, dedicated analog input pair, the internal junction temperature sensing diode and internal voltage rails. The input signal can be converted in either uni-polar or bi-polar mode.

The reference voltage is selectable between the 1.2 V internal reference generator and an external reference. The ADC can convert up to a 1.8 V input signal with a 1.8 V external reference voltage. The ADC has an auto-calibration function which calibrates the gain and offset.

2.13.2. Continuous Time Comparators

The continuous-time comparator can be used to compare a pre-selected GPIO's input pairs or one dedicated comparator input pair. The output of the comparator is provided as continuous and latched data.

2.13.3. Internal Junction Temperature Monitoring Diode

On-die junction temperature can be monitored using the internal junction temperature monitoring diode. The PTAT (proportional to absolute temperature) diode voltage can be monitored by the ADC to provide a digital temperature readout. Refer to CrossLink-NX ADC Usage Guide (FPGA-TN-02129) for more details.

2.14. IEEE 1149.1-Compliant Boundary Scan Testability

All CrossLink-NX devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/O: TDI, TDO, TCK, and TMS. The test access port uses VCCIO1 for power supply. The test access port is supported for VCCIO1 = 1.8 V - 3.3 V.

For more information, refer to CrossLink-NX sysCONFIG Usage Guide (FPGA-TN-02099).

2.15. Device Configuration

All CrossLink-NX devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration, and the sysCONFIG port, support serial, quad, and byte configuration. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. The JTAG_EN is the only dedicated pin supported by *sysCONFIG. PPROGRAMN/INITN/DONE* are enabled by default, but can be turned into GPIO. The remaining sysCONFIG pins are used as dual function pins. Refer to CrossLink-NX sysCONFIG Usage Guide (FPGA-TN-02099) for more information about using the dual-use pins as general purpose I/O.

There are various ways to configure a CrossLink-NX device:

- JTAG
- Standard Serial Peripheral Interface (SPI) – Interface to boot PROM Support x1, x2, x4 wide SPI memory interfaces. (Master SPI mode)
- Inter-Integrated Circuit Bus (I^2C)
- Improved Inter-Integrated Circuit Bus (I3C)
- System microprocessor to drive a serial slave SPI port (SSPI mode)

- Lattice Memory Mapped Interface (LMMI), refer to CrossLink-NX sysI/O Usage Guide (FPGA-TN-02067) for condition.
- JTAG, SSPI, MSPI, I^2C, and I3C are supported for VCCIO = 1.8 V - 3.3 V

On power-up, based on the voltage level (high or low) of the PROGRAMN pin the FPGA SRAM is configured by the appropriate sysCONFIG port. If PROGRAMN pin is *low*, the FPGA is in the Slave configuration ports (Slave SPI, Slave I^2C or Slave I3C) and is waiting for the correct Slave Configuration port activation key. PROGRAMN pin must be driven high within 50 ns of the end of transmission of the Slave Configuration port activation key, that is, the de-assertion of SCSN. If no slave port is declared active before the PROGRAMN pin is sensed HIGH, the FPGA is in Master SPI booting sequence (mode). In Master SPI booting mode, the FPGA boots from an external SPI boot PROM. Once a configuration port is activated, it remains active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by enabling the JTAG_EN pin and sending the appropriate command through the TAP port.

2.15.1. Enhanced Configuration Options

CrossLink-NX devices have enhanced configuration features such as:

- Early I/O release
- Bitstream Decryption
- Decompression Support
- Watchdog Timer support
- Dual and Multi-boot image support

Early I/O Release is a new configuration feature in which certain I/O banks are released earlier so that customer systems have minimal disruption. For more details, refer to CrossLink-NX sysCONFIG Usage Guide (FPGA-TN-02099).

Watchdog Timer is a new configuration feature that helps you add a programmable timer option for timeout applications.

2.15.2.1. Dual-Boot and Multi-Boot Image Support

Dual-boot and multi-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the CrossLink-NX devices can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the CrossLink-NX device can revert back to the original backup golden configuration and try again. This all can be done without power cycling the system. For more information, refer to CrossLink-NX sysCONFIG Usage Guide (FPGA-TN-02099).

2.16. Single Event Upset (SEU) Support

CrossLink-NX devices are unique due to the underlying technology used to build these devices is much more robust and less prone to soft errors.

CrossLink-NX devices have an improved hardware implemented Soft Error Detection (SED) circuit which can be used to detect SRAM errors and allow them to be corrected. There are two layers of SED implemented in CrossLink-NX making it more robust and reliable.

The SED hardware in CrossLink-NX devices is part of the Configuration block. The SED module in CrossLink-NX is an enhanced version as compared to the SED modules implemented in other Lattice devices. The configuration data is divided into frames so that the entire FPGA can be programmed precisely with ease. The SED hardware reads data from the FPGAs configuration memory and performs Error Correcting Code (ECC) calculation on every frame of configuration data (see Figure 2.1). Once a single bit of error is detected, Soft Error Upset (SEU), a notification is generated and SED resumes operation. For single bit errors, the corrected value is rewritten to the particular frame using ECC information. If more than one-bit error is detected within one frame of configuration data, an error message is generated. CrossLink-NX devices also have a dedicated logic to perform Cycle Redundancy Code (CRC) checks. This CRC runs in parallel for the entire bitstream along with ECC.

After the ECC is calculated on all frames of configuration data, Cyclic Redundancy Check (CRC) is calculated for the entire configuration data (bitstream). The data that is read, and the ECC and CRC calculated, do not include EBR Big SRAM and distributed RAM memory.

For further information on SED support, refer to CrossLink-NX Soft Error Detection (SED)/Correction (SEC) Usage Guide (FPGA-TN-02076).

2.17. On-Chip Oscillator

The CrossLink-NX device features two different frequency Oscillators. One is tailored for low-power operation that runs at low frequency (LFOSC). Both Oscillators are controlled with internally generated current.

The LFOSC runs at nominal frequency of 128 kHz. The high frequency oscillator (HFOSC) runs at a nominal frequency of 450 MHz, and can be divisible from 2 to 256 for output frequency between 1.758 MHz (div256) and 225 MHz (div2). The LFOSC always run, thus can be used to perform all always-on functions with the lowest power possible.

2.18. User I²C IP

The CrossLink-NX device has one I²C IP core. The core can be configured either as an I²C master or as an I²C slave. The pins for the I²C interface are pre-assigned.

The core has the option to delay the either the input or the output, or both, by 50 ns nominal, using dedicated on-chip delay elements. This provides an easier interface with any external I²C components. In addition, 50 ns glitch filters are available for both SDA and SCL.

When the IP core is configured as master, it is able to control other devices on the I²C bus through the pre-assigned pin interface. When the core is configured as the slave, the device is able to provide, for example, I/O expansion to an I²C Master. The I²C core supports the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Clock stretching
- Up to 1 MHz data transfer speed (Standard-Mode, Fast-Mode, Fast-Mode Plus)
- General Call support
- Optional receive and transmit data FIFOs with programmable sizes
- Optionally 50 ns delay on input or output data, or both
- Hard-Connection and Programmable I/O Connection Support
- Programmable to a mode compliant with I3C requirements on legacy I²C Slave Devices.
- Fast-Mode and Fast-Mode Plus Support

- Disabled Clock Stretching
- 50 ns SCL and SDA Glitch Filter
- Programmable 7-bit Address

For further information on the User I²C, refer to CrossLink-NX I²C Hardened IP Usage Guide (FPGA-TN-02142).

2.19. Density Shifting

The CrossLink-NX family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization impact the likelihood of success in each case. An example is that some user I/O may become No Connects in smaller devices in the same package. Refer to the CrossLink-NX Pin Migration Tables and Lattice Radiant software for specific restrictions and limitations.

2.20. MIPI D-PHY Blocks

The top side of the device includes two Hardened MIPI D-PHY quads. The Hardened D-PHY can be configured to support either Camera Serial Interface (CSI-2) or Display Serial Interface (DSI) applications as either transmitter or receiver. Below is a summary of the features supported by the Hardened D-PHY quads.

- Transmit and receive compliant to MIPI Alliance's MIPI D-PHY Specification version 1.2
- High-Speed (HS) and Low-Power (LP) mode support (including build-in contention detection)
- Supports continuous clock mode or low power (non-continuous) clock mode
- Up to 10 Gbps per quad (2500 Mbps data rate per lane)
- Supports up to 4 data lanes and one clock lane per Hardened D-PHY

CrossLink-NX's programmable I/O can also be configured as MIPI D-PHYs, referred to as Soft MIPI D-PHY. The Soft D-PHY can be configured to support either Camera Serial Interface (CSI-2) or Display Serial Interface (DSI) applications as either transmitter or receiver. Below is a summary of the features supported by the Soft D-PHY.

- Transmit and receive compatible to MIPI Alliance's MIPI D-PHY Specification version 1.1
- High-Speed (HS) and Low-Power (LP) mode support (does not support contention detection)
- Supports continuous clock mode or low power (non-continuous) clock mode
- Up to 6 Gbps per port (1500 Mbps data rate per lane) in 121 csfBGA package
- Up to 5 Gbps per port (1250 Mbps data rate per lane) in other packages
- Supports up to 4 data lanes and one clock lane per port

2.21. Peripheral Component Interconnect Express (PCIe)

The CrossLink-NX-40 Device features one lane of hardened PCIe block on the top side of the device. The PCIe block implements all three layers defined by the PCI Express Specification: Physical, Data Link, and Transaction as shown in Figure 2.28. Below is a summary of the features supported by the PCIe:

- Gen 1 (2.5 Gb/s) and Gen 2 (5.0 Gb/s) speed
- PCIe Express Base Specification 3.0 compliant including compliance with earlier PCI Express Specifications
- Multi-function support with up to four physical functions
- Endpoint and root complex support
- Type 0 Configuration Registers in Endpoint Mode
- Complete Error-Handling Support
- 32-bit Core Data Width
- Many power management features including power budgeting

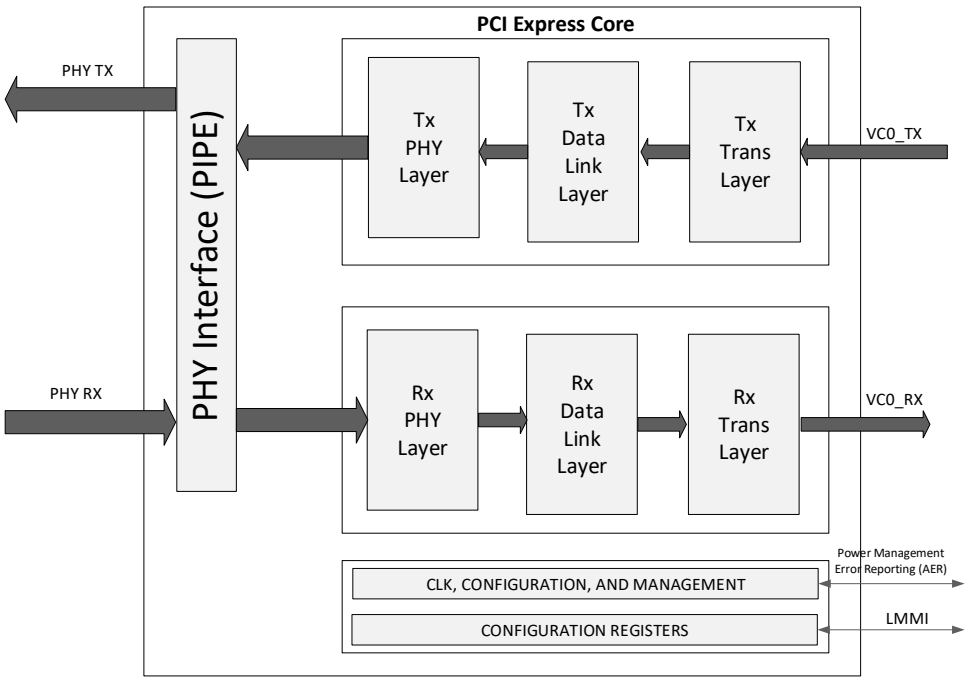


Figure 2.28. PCIe Core

The hardened PCIe block can be instantiated with the primitive *PCIe* through Lattice Radiant software however, it is not recommended to directly instantiate the PCIe primitive itself. It is highly recommended to generate the PCIe Endpoint Soft IP through IP Express instead. In Figure 2.29, the PCIe core is configured as Endpoint using the Soft logic and this Endpoint soft IP provides a wrapper around the PCIe primitive as well as providing useful functions such as bridging support for bus interfaces and DMA applications. In addition to the standard Transaction Layer Packet (TLP) interface, the data interface can also be configured to be AXI4 or AHB-Lite interfaces as well. The PCIe hardened block also features a register interface of LMMI and User Configuration Space Register Interface (UCFG). With the soft IP, the interface can be configured to APB or AHB-Lite as well. The PCIe block contains many registers which contains information about the current status of the PCIe block as well as the capability to dynamically switch PCIe settings. One easy way to access these registers is through the Reveal Controller Tool.

For more information about the PCIe soft IP, refer to the PCIe Endpoint IP Core document.

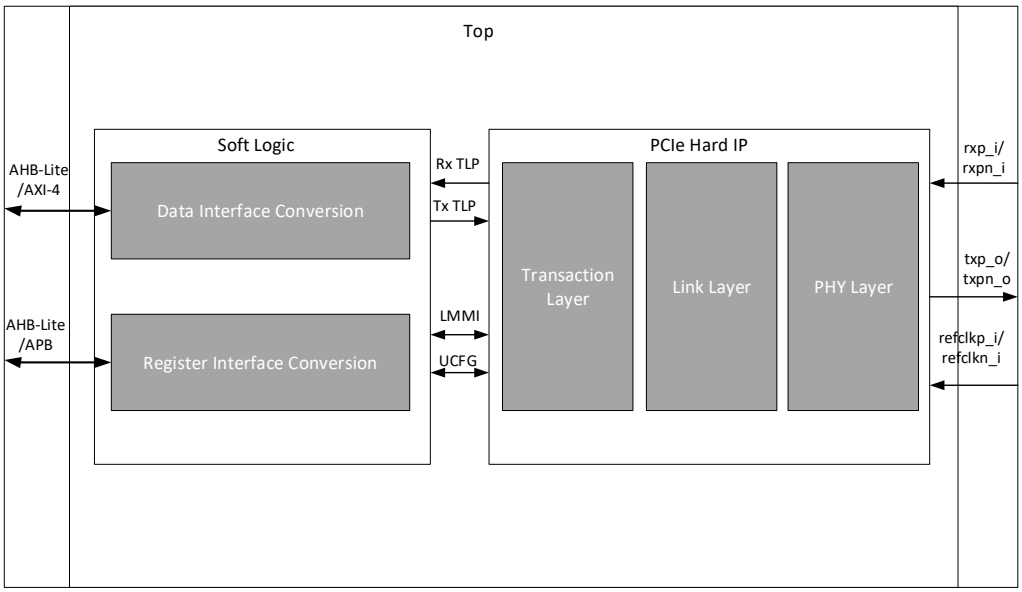


Figure 2.29. PCIe Soft IP Wrapper

2.22. Cryptographic Engine

The CrossLink-NX family of devices support several cryptographic features that helps customer secure their design. Some of the key cryptographic features include Advanced Encryption Standard (AES), Hashing Algorithms and true random number generator (TRNG). The CrossLink-NX device also features bitstream encryption (using AES-256) and bitstream authentication (using ECDSA), which protects the FPGA design bitstream from copying and tampering.

The Cryptographic Engine (CRE) is the main engine, which is responsible for the bitstream encryption as well as authentication of the CrossLink-NX device. Once the bitstream is authenticated and the device is ready for user functions, the CRE is available for you to implement various cryptographic functions in your FPGA design. To enable specific cryptographic function, the CRE has to be configured by setting a few registers.

The Cryptographic Engine supports the below user-mode features:

- True Random Number generator (TRNG)
- Secure Hashing Algorithm (SHA)-256 bit
- Message authentication codes (MACs) – HMAC
- Lattice Memory Mapped Interface (LMMI) interface to user logic
- High Speed Port (HSP) for FIFO-based streaming data transfer

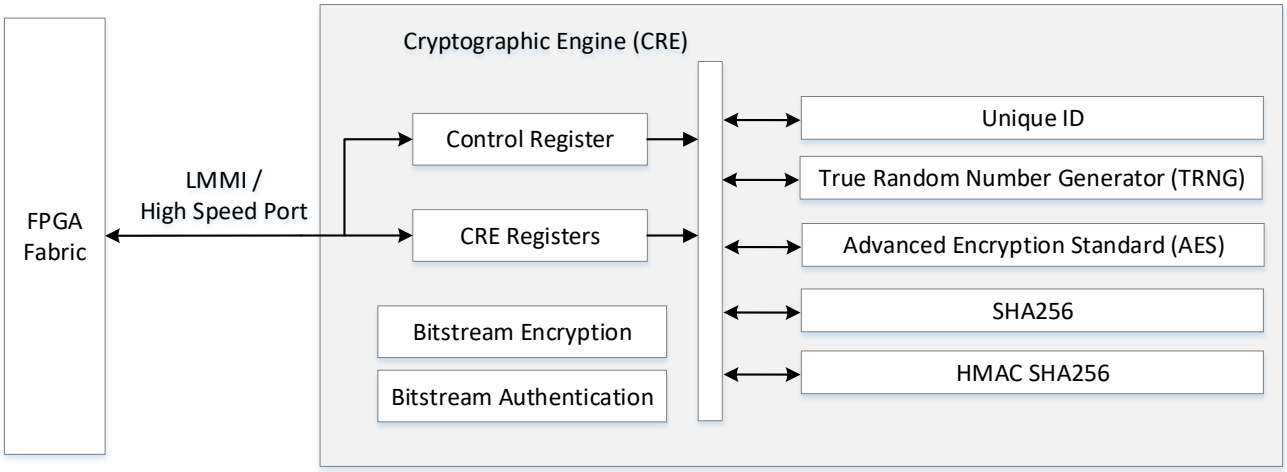


Figure 2.30. Cryptographic Engine Block Diagram

3. DC and Switching Characteristics for Commercial and Industrial

3.1. Absolute Maximum Ratings

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CC}, V_{CCECLK}	Supply Voltage	–0.5	1.10	V
V_{CCAUX}, V_{CCAUXA}, $V_{CCAUXH3}$, $V_{CCAUXH4}$, $V_{CCAUXH5}$	Supply Voltage	–0.5	1.98	V
$V_{CCIO0, 1, 2, 6, 7}$	I/O Supply Voltage	–0.5	3.63	V
$V_{CCIO3, 4, 5}$	I/O Supply Voltage	–0.5	1.98	V
$V_{CCPLL\_DPHY0, 1}$	Hardened D-PHY PLL Supply Voltage	–0.5	1.10	V
$V_{CCPLLSD0}$	SerDes Block PLL Supply Voltage	–0.5	1.98	V
$V_{CCA\_DPHY0, 1}$	Analog Supply Voltage for Hardened D-PHY	–0.5	1.98	V
$V_{CC\_DPHY0, 1}$	Digital Supply Voltage for Hardened D-PHY	–0.5	1.10	V
V_{CCSD0}	SerDes Supply Voltage	–0.5	1.10	V
$V_{CCADC18}$	ADC Block 1.8 V Supply Voltage	–0.5	1.98	V
$V_{CCAUXSD}$	SerDes and AUX Supply Voltage	–0.5	1.98	V
—	Input or I/O Voltage Applied, Bank 0, Bank 1,Bank 2, Bank 6, Bank 7	–0.5	3.63	V
—	Input or I/O Voltage Applied, Bank 3, Bank 4, Bank 5	–0.5	1.98	V
—	Voltage Applied on SerDes Pins	–0.5	1.98	V
T_A	Storage Temperature (Ambient)	–65	150	°C
T_J	Junction Temperature	—	+125	°C

Notes:

1. Stress above those listed under the *Absolute Maximum Ratings* may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. All V_{CCAUX} should be connected on PCB.

3.2. Recommended Operating Conditions[1, 2, 3]

Table 3.2. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
V_{CC}, V_{CCECLK}	Core Supply Voltage	V_{CC} = 1.0	0.95	1.00	1.05	V
V_{CCAUX}	Auxiliary Supply Voltage	Bank 0, Bank 1, Bank 2, Bank 6, Bank 7	1.746	1.80	1.89	V
$V_{CCAUXH3/4/5}$	Auxiliary Supply Voltage	Bank 3, Bank 4, Bank 5	1.746	1.80	1.89	V
V_{CCAUXA}	Auxiliary Supply Voltage for core logic	—	1.746	1.80	1.89	V
V_{CCIO}	I/O Driver Supply Voltage	V_{CCIO} = 3.3 V, Bank 0, Bank 1, Bank 2, Bank 6, Bank 7	3.135	3.30	3.465	V
		V_{CCIO} = 2.5 V, Bank 0, Bank 1, Bank 2, Bank 6, Bank 7	2.375	2.50	2.625	V
		V_{CCIO} = 1.8 V, All Banks	1.71	1.80	1.89	V
		V_{CCIO} = 1.5 V, All Banks[4]	1.425	1.50	1.575	V
		V_{CCIO} = 1.35 V, All Banks (For DDR3L Only)	1.2825	1.35	1.4175	V
		V_{CCIO} = 1.2 V, All Banks[4]	1.14	1.20	1.26	V
		V_{CCIO} = 1.0 V, Bank 3, Bank 4, Bank 5	0.95	1.00	1.05	V
D-PHY External Power Supplies						
$V_{CCA\_D\text{-}PHY}$	D-PHY Analog Power Supply	—	1.71	1.80	1.89	V
$V_{CC\_D\text{-}PHY}$	D-PHY Digital Power Supply	—	0.95	1.00	1.05	V
$V_{CCPLL\_D\text{-}PHY}$	D-PHY PLL Power Supply	—	0.95	1.00	1.05	V
ADC External Power Supplies						
$V_{CCADC18}$	ADC 1.8 V Power Supply	—	1.71	1.80	1.89	V
SerDes Block External Power Supplies						
V_{CCSD0}	Supply Voltage for SerDes Block and SerDes I/O	—	0.95	1.00	1.05	V
$V_{CCPLLSD0}$	SerDes Block PLL Supply Voltage	—	1.71	1.80	1.89	V
$V_{CCAUXSD}$	SerDes Block Auxiliary Supply Voltage	—	1.71	1.80	1.89	V
Operating Temperature						
t_{JCOM}	Junction Temperature, Commercial Operation	—	0	—	85	°C
t_{JIND}	Junction Temperature, Industrial Operation	—	–40	—	100	°C

Notes:

1. For correct operation, all supplies must be held in their valid operation voltage range.
2. All supplies with same voltage should be from the same voltage source. Proper isolation filters are needed to properly isolate noise from each other.
3. Common supply rails must be tied together except SerDes.
4. MSPI (Bank0) and JTAG, SSPI, I^2C, and I3C (Bank 1) ports are supported for V_{CCIO} = 1.8 V to 3.3 V.

3.3. Power Supply Ramp Rates

Table 3.3. Power Supply Ramp Rates

Symbol	Parameter	Min	Typ	Max	Unit
t_{RAMP}	Power Supply ramp rates for all supplies [1]	0.1	—	50	V/ms

Notes:

1. Assumes monotonic ramp rates.
2. All supplies need to be in the operating range as defined in Recommended Operating Conditions1, when the device has completed configuration and entering into User Mode. Supplies that are not in the operating range needs to be adjusted to faster ramp rate, or you have to delay configuration or wake up.

3.4. Power up Sequence

Power-On-Reset (POR) puts the CrossLink-NX device into a reset state. There is no power up sequence required for the CrossLink-NX device.

Table 3.4. Power-On Reset

Symbol	Parameter		Min	Typ	Max	Unit
V_{PORUP}	Power-On-Reset ramp-up trip point (Monitoring V_{CC}, V_{CCAUX}, V_{CCIO0}, and V_{CCIO1})	V_{CC}	0.73	—	0.83	V
		V_{CCAUX}	1.34	—	1.71	V
		V_{CCIO0},V_{CCIO1}	0.89	—	1.05	V
V_{PORDN}	Power-On-Reset ramp-up trip point (Monitoring V_{CC} and V_{CCAUX})	V_{CC}	0.51	—	0.81	V
		V_{CCAUX}	1.38	—	1.54	V

3.5. On-Chip Programmable Termination

The CrossLink-NX devices support a variety of programmable on-chip terminations options, including:

- Dynamically switchable Single-Ended Termination with programmable resistor values of 40 Ω, 50 Ω, 60 Ω, or 75 Ω.
- Common mode termination of 100 Ω for differential inputs.

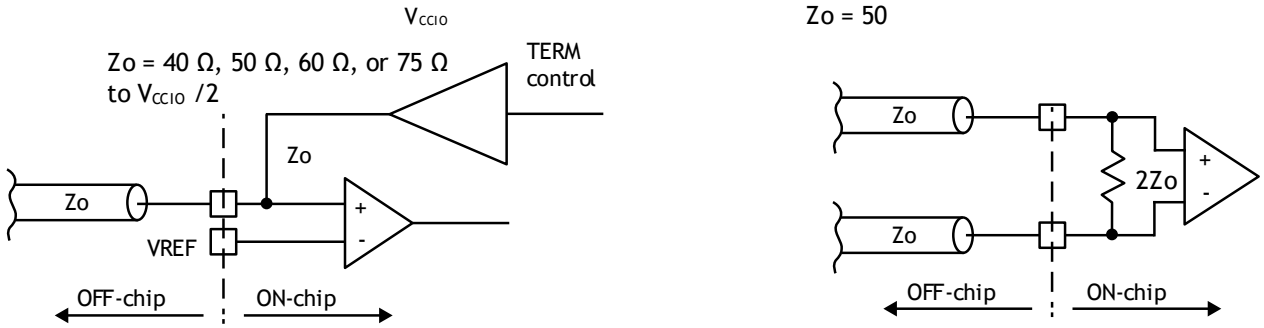


Figure 3.1. On-Chip Termination

See Table 3.5 for termination options for input modes.

Table 3.5. On-Chip Termination Options for Input Modes

IO_TYPE	Differential Termination Resistor*	Terminate to $V_{CCIO}/2$*
subLVDS	100, OFF	OFF
SLVS	100, OFF	OFF
MIPI_DPHY	100	OFF
HSTL15D_I	100, OFF	OFF

IO_TYPE	Differential Termination Resistor*	Terminate to $V_{CCIO}/2$*
SSTL15D_I	100, OFF	OFF
SSTL135D_I	100, OFF	OFF
HSUL12D	100, OFF	OFF
LVCMOS15H	OFF	OFF
LVCMOS12H	OFF	OFF
LVCMOS10H	OFF	OFF
LVCMOS12H	OFF	OFF
LVCMOS10H	OFF	OFF
LVCMOS18H	OFF	OFF, 40, 50, 60, 75
HSTL15_I	OFF	50
SSTL15_I	OFF	OFF, 40, 50, 60, 75
SSTL135_I	OFF	OFF, 40, 50, 60, 75
HSUL12	OFF	OFF, 40, 50, 60, 75

*Notes:

- TERMINATE to $V_{CCIO}/2$ (Single-Ended) and DIFFRENTIAL TERMINATION RESISTOR when turned on can only have one setting per bank. Only left and right banks have this feature.
- Use of TERMINATE to $V_{CCIO}/2$ and DIFFRENTIAL TERMINATION RESISTOR are mutually exclusive in an I/O bank. On-chip termination tolerance –10%/+60%.

Refer to CrossLink-NX sysI/O Usage Guide (FPGA-TN-02067) for on-chip termination usage and value ranges.

3.6. Hot Socketing Specifications

Table 3.6. Hot Socketing Specifications for GPIO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DK}	Input or I/O Leakage Current for Wide Range I/O (excluding MCLK/MCSN/MOSI/INITN/DONE)	0 < Vin < Vih(max) 0 < Vcc < Vcc(max) 0 < Vccio < Vccio(max) 0 < Vccaux < Vccaux(max)	-1.5	—	1.5	mA

Notes:

- I_{DK} is additive to I_{PU}, I_{PW}, or I_{BH}.
- Hot socket specification defines when the hot socketed device's junction temperature is at 85 °C or below. When the hot socketed device's junction temperature is above 85 °C, the I_{DK} current can exceed the above spec.
- Going beyond the hot socketing ranges specified here will cause exponentially higher Leakage currents and potential reliability issues. A total of 64mA per 8 I/O should not be exceeded.

3.7. ESD Performance

Refer to the CrossLink-NX Product Family Qualification Summary for complete qualification data, including ESD performance.

3.8. DC Electrical Characteristics

Table 3.7. DC Electrical Characteristics – Wide Range (Over Recommended Operating Conditions)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IL}, I_{IH}[1]	Input or I/O Leakage current (Commercial/Industrial)	$0 \le V_{IN} \le V_{CCIO}$	—	—	10	µA
I_{IH}[2]	Input or I/O Leakage current	$V_{CCIO} \le V_{IN} \le V_{IH}$ (max)	—	—	100	µA
I_{PU}	I/O Weak Pull-up Resistor Current	$0 \le V_{IN} \le 0.7 * V_{CCIO}$	–30	—	–150	µA
I_{PD}	I/O Weak Pull-down Resistor Current	V_{IL} (max) $\le V_{IN} \le V_{CCIO}$	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (max)	30	—		µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7 * V_{CCIO}$	–30	—		µA
I_{BHLO}	Bus hold low Overdrive Current	$0 \le V_{IN} \le V_{CCIO}$	—	—	150	µA
I_{BHHO}	Bus hold high Overdrive Current	$0 \le V_{IN} \le V_{CCIO}$	—	—	–150	µA
V_{BHT}	Bus Hold Trip Points	—	V_{IL} (max)	—	V_{IH} (min)	V

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output tristated. Bus Maintenance circuits are disabled.
2. The input leakage current I_{IH} is the worst case input leakage per GPIO when the pad signal is high and also higher than the bank V_{CCIO}. This is considered a mixed mode input.

Table 3.8. DC Electrical Characteristics – High Speed (Over Recommended Operating Conditions)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IL}, I_{IH}[1]	Input or I/O Leakage	$0 \le V_{IN} \le V_{CCIO}$	—	—	10	µA
I_{PU}	I/O Weak Pull-up Resistor Current	$0 \le V_{IN} \le 0.7 * V_{CCIO}$	–30	—	–150	µA
I_{PD}	I/O Weak Pull-down Resistor Current	V_{IL} (max) $\le V_{IN} \le V_{CCIO}$	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (max)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7 * V_{CCIO}$	–30	—	—	µA
I_{BHLO}	Bus hold low Overdrive Current	$0 \le V_{IN} \le V_{CCIO}$	—	—	150	µA
I_{BHHO}	Bus hold high Overdrive Current	$0 \le V_{IN} \le V_{CCIO}$	—	—	–150	µA
V_{BHT}	Bus Hold Trip Points	—	V_{IL} (max)	—	V_{IH} (min)	V

Note: Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output tristated. Bus Maintenance circuits are disabled.

Table 3.9. Capacitors – Wide Range (Over Recommended Operating Conditions)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
C_1*	I/O Capacitance*	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = typ., V_{IO} = 0 to V_{CCIO} + 0.2V	—	6	—	pf
C_2*	Dedicated Input Capacitance*	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = typ., V_{IO} = 0 to V_{CCIO} + 0.2V	—	6	—	pf

*__Note__: T_A 25 °C, f = 1.0 MHz.

Table 3.10. Capacitors – High Performance (Over Recommended Operating Conditions)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
C_1*	I/O Capacitance*	V_{CCIO} = 1.8 V, 1.5 V, 1.2 V, V_{CC} = typ., V_{IO} = 0 to V_{CCIO} + 0.2V	—	6	—	pf
C_2*	Dedicated Input Capacitance*	V_{CCIO} = 1.8 V, 1.5 V, 1.2 V, V_{CC} = typ., V_{IO} = 0 to V_{CCIO} + 0.2V	—	6	—	pf

Symbol	Parameter	Condition	Min	Typ	Max	Unit
C_3*	D-PHY I/O Capacitance	$V_{CCA\_D\text{-}PHY}$ = 1.8 V, V_{CC} = typ., V_{IO} = 0 to $V_{CCA\_D\text{-}PHY}$ + 0.2V	—	5	—	pf
C_4*	SerDes I/O Capacitance	V_{CCSD0} = 1.0 V, V_{CC} = typ., V_{IO} = 0 to V_{CCSD0} + 0.2 V	—	5	—	pf

*Note: T_A 25 °C, f = 1.0 MHz.

Table 3.11. Single Ended Input Hysteresis – Wide Range (Over Recommended Operating Conditions)

IO_TYPE	VCCIO	TYP Hysteresis
LVCMOS33	3.3 V	250 mV
LVCMOS25	3.3 V	200 mV
	2.5 V	250 mV
LVCMOS18	1.8 V	180 mV
LVCMOS15	1.5 V	50 mV
LVCMOS12	1.2 V	0
LVCMOS10	1.2 V	0

Table 3.12. Single Ended Input Hysteresis – High Performance (Over Recommended Operating Conditions)

IO_TYPE	VCCIO	TYP Hysteresis
LVCMOS18H	1.8 V	180 mV
LVCMOS15H	1.8 V	50 mV
	1.5 V	150 mV
LVCMOS12H	1.2 V	0
LVCMOS10H	1.0 V	0
MIPI-LP-RX	1.2 V	>25 mV

3.9. Supply Currents

For estimating and calculating current, use Power Calculator in Lattice Design Software.

This operating and peak current is design dependent, and can be calculated in Lattice Design Software. Some blocks can be placed into low current standby modes. Refer to Power Management and Calculation for CrossLink-NX Devices (FPGA-TN-02075).

3.10. sysI/O Recommended Operating Conditions

Table 3.13. sysI/O Recommended Operating Conditions

Standard	Support Banks	V_{CCIO} (Input)	V_{CCIO} (Output)
		Typ.	Typ.
Single-Ended			
LVCMOS33	0, 1, 2, 6, 7	3.3	3.3
LVTTL33	0, 1, 2, 6, 7	3.3	3.3
LVCMOS25[1, 2]	0, 1, 2, 6, 7	2.5, 3.3	2.5
LVCMOS18[1, 2]	0, 1, 2, 6, 7	1.2, 1.5, 1.8, 2.5, 3.3	1.8
LVCMOS18H	3, 4, 5	1.8	1.8
LVCMOS15[1, 2]	0, 1, 2, 6, 7	1.2, 1.5, 1.8, 2.5, 3.3	1.5
LVCMOS15H[1]	3, 4, 5	1.5, 1.8	1.5
LVCMOS12[1, 2]	0, 1, 2, 6, 7	1.2, 1.5, 1.8, 2.5, 3.3	1.2
LVCMOS12H[1]	3, 4, 5	1.2, 1.35[7], 1.5, 1.8	1.2
LVCMOS10[1]	0, 1, 2, 6, 7	1.2, 1.5, 1.8, 2.5, 3.3	—
LVCMOS10H[1]	3, 4, 5	1.0, 1.2, 1.35[7], 1.5, 1.8	1.0
LVCMOS10R[1]	3, 4, 5	1.0, 1.2, 1.35[7], 1.5, 1.8	—
SSTL135_I, SSTL135_II[3]	3, 4, 5	1.35[7]	1.35
SSTL15_I, SSTL15_II[3]	3, 4, 5	1.5[8]	1.5[8]
HSTL15_I[3]	3, 4, 5	1.5[8]	1.5[8]
HSUL12[3]	3, 4, 5	1.2	1.2
MIPI D-PHY LP Input[3, 6]	3, 4, 5	1.2	1.2
Differential[6]			
LVDS	3, 4, 5	1.8	1.8
LVDSE[5]	0, 1, 2, 6, 7	—	2.5
subLVDS	3, 4, 5	1.8	—
subLVDSE[5]	0, 1, 2, 6, 7	—	1.8
subLVDSEH[5]	3, 4, 5	—	1.8
SLVS[6]	3, 4, 5	1.0, 1.2, 1.35[7], 1.5, 1.8[4]	1.2, 1.35[7], 1.5, 1.8 [4]
MIPI D-PHY[6]	3, 4, 5	1.2	1.2
LVCMOS33D[5]	0, 1, 2, 6, 7	—	3.3
LVTTL33D[5]	0, 1, 2, 6, 7	—	3.3
LVCMOS25D[5]	0, 1, 2, 6, 7	—	2.5
SSTL135D_I, SSTL135D_II[5]	3, 4, 5	—	1.35[7]
SSTL15D_I, SSTL15D_II[5]	3, 4, 5	—	1.5
HSTL15D_I[5]	3, 4, 5	—	1.5
HSUL12D[5]	3, 4, 5	—	1.2

Notes:

1. Single-ended input can mix into I/O Banks with V_{CCIO} different from the standard requires due to some of these input standards use internal supply voltage source (V_{CC}, V_{CCAUX}) to power the input buffer, which makes them to be independent of V_{CCIO} voltage. For more details, please refer to CrossLink-NX sysI/O Usage Guide (FPGA-TN-02067). The following is a brief guideline to follow:
   a. Weak pull-up on the I/O must be set to OFF.
   b. Bank 3, Bank 4, and Bank 5 I/O can only mix into banks with V_{CCIO} higher than the pin standard, due to clamping diode on the pin in these banks. Bank 0, Bank 1, Bank 2, Bank 6, and Bank 7 does not have this restriction.
   c. LVCMOS25 uses V_{CCIO} supply on input buffer in Bank 0, Bank 1, Bank 2, Bank 6, and Bank 7. It can be supported with V_{CCIO} = 3.3 V to meet the V_{IH} and V_{IL} requirements, but there is additional current drawn on V_{CCIO}. Hysteresis has to be disabled when using 3.3 V supply voltage.
   d. LVCMOS15 uses V_{CCIO} supply on input buffer in Bank 3, Bank 4, and Bank 5. It can be supported with V_{CCIO} = 1.8 V to meet the V_{IH} and V_{IL} requirements, but there is additional current drawn on V_{CCIO}.

2. Single-ended LVCMOS inputs can mixed into I/O Banks with different V_{CCIO}, providing weak pull-up is not used. For additional information on Mixed I/O in Bank V_{CCIO}, refer to CrossLink-NX sysI/O Usage Guide (FPGA-TN-02067).
3. These inputs use differential input comparator in Bank 3, Bank 4, and Bank 5. The differential input comparator uses V_{CCAUXH} power supply. These inputs require the V_{REF} pin to provide the reference voltage in the Bank. Refer to CrossLink-NX sysI/O Usage Guide (FPGA-TN-02067) for details.
4. All differential inputs use differential input comparator in Bank 3, Bank 4, and Bank 5. The differential input comparator uses V_{CCAUXH} power supply. There is no differential input signaling supported in Bank 0, Bank 1, Bank 2, Bank 6, and Bank 7.
5. These outputs are emulating differential output pair with single-ended output drivers with true and complement outputs driving on each of the corresponding true and complement output pair pins. The common mode voltage, V_{CM}, is ½ * V_{CCIO}. Refer to CrossLink-NX sysI/O Usage Guide (FPGA-TN-02067) for details.
6. Soft MIPI D-PHY HS using sysI/O is supported with SLVS input and output that can be placed in banks with V_{CCIO} voltage shown in SLVS. D-PHY with HS and LP modes supported needs to be placed in banks with V_{CCIO} voltage = 1.2 V. Soft MIPI D-PHY LP input and output using sysI/O are supported with LVCMOS12.
7. V_{CCIO} = 1.35 V is only supported in Bank 3, Bank 4, and Bank 5, for use with DDR3L interface in the bank. These Input and Output standards can fit into the same bank with the V_{CCIO} = 1.35 V.
8. LVCMOS15 input uses V_{CCIO} supply voltage. If V_{CCIO} is 1.8 V, the DC levels for LVCMOS15 are still met, but there could be increase in input buffer current.

3.11. sysI/O Single-Ended DC Electrical Characteristics

Table 3.14. sysI/O DC Electrical Characteristics – Wide Range I/O (Over Recommended Operating Conditions)

Input/Output Standard	V_{IL}[1]		V_{IH}[1]		V_{OL} Max (V)	V_{OH} Min[2] (V)	I_{OL}(mA)	I_{OH}(mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVTTL33 LVCMOS33	—	0.8	2.0	3.465	0.4	V_{CCIO} – 0.4	2, 4, 8, 12, 16	-2, -4, -8, -12, -16
LVCMOS25	—	0.7	1.7	2.625	0.4	V_{CCIO} – 0.45	2, 4, 8, 10	-2, -4, -8, -10
LVCMOS18	—	0.35 * V_{CCIO}	0.65 * V_{CCIO}	1.9	0.4	V_{CCIO} – 0.45	2, 4, 8	-2, -4, -8
LVCMOS15	—	0.35 * V_{CCIO}	0.65 * V_{CCIO}	1.575	0.4	V_{CCIO} – 0.4	2, 4	-2, -4
LVCMOS12	—	0.35 * V_{CCIO}	0.65 * V_{CCIO}	1.26	0.4	V_{CCIO} – 0.4	2, 4	-2, -4, -8, -12
LVCMOS10	—	0.3 * V_{CCIO}	0.7 * V_{CCIO}	1.05	No O/P Support			

Notes:
1. V_{CCIO} for input level refers to the supply rail level associated with a given input standard or the upstream driver V_{CCIO} rail levels.
2. V_{CCIO} for the output levels refer to the V_{CCIO} of the CrossLink-NX device.

Table 3.15. sysI/O DC Electrical Characteristics – High Performance I/O (Over Recommended Operating Conditions)

Input/Output Standard	V_{IL}[1]		V_{IH}[1]		V_{OL} Max (V)	V_{OH} Min[2] (V)	I_{OL} (mA)	I_{OH} (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS18H		0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.4	V_{CCIO} – 0.45	2, 4, 8, 12	-2, -4, -8, -12
LVCMOS15H		0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.4	V_{CCIO} – 0.4	2, 4, 8	-2, -4, -8
LVCMOS12H		0.35 * V_{CCIO}	0.65 * V_{CCIO}	1.26	0.4	V_{CCIO} – 0.4	2, 4, 8	-2, -4, -8
LVCMOS10H		0.3 * V_{CCIO}	0.7 * V_{CCIO}	1.05	0.27 * V_{CCIO}	0.75 * V_{CCIO}	2, 4	-2, -4
SSTL15_I		V_{REF} – 0.10	V_{REF} + 0.1	1.575	0.30	V_{CCIO} – 0.30	7.5	–7.5
SSTL15_II		V_{REF} – 0.10	V_{REF} + 0.1	1.575	0.30	V_{CCIO} – 0.30	8.8	–8.8
HSTL15_I		V_{REF} – 0.10	V_{REF} + 0.1	1.575	0.40	V_{CCIO} – 0.40	8	–8
SSTL135_I		V_{REF} – 0.09	V_{REF} + 0.09	1.418	0.27	V_{CCIO} – 0.27	6.75	–6.75
SSTL135_II		V_{REF} – 0.09	V_{REF} + 0.09	1.418	0.27	V_{CCIO} – 0.27	8	–8
LVCMOS10R		V_{REF} – 0.10	V_{REF} + 0.10	1.05	—	—	—	—
HSUL12		V_{REF} – 0.10	V_{REF} + 0.10	1.26	0.3	V_{CCIO} – 0.3	8.8, 7.5, 6.25, 5	-8.8, -7.5, -6.25, -5

Notes:
1. V_{CCIO} for input level refers to the supply rail level associated with a given input standard or the upstream driver V_{CCIO} rail levels.
2. V_{CCIO} for the output levels refer to the V_{CCIO} of the CrossLink-NX device.

Table 3.16. I/O Resistance Characteristics (Over Recommended Operating Conditions)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
50RS	Output Drive Resistance when 50RS Drive Strength Selected	V_{CCIO} = 1.8 V, 2.5 V, or 3.3 V	—	50	—	Ω
R_{DIFF}	Input Differential Termination Resistance	Bank 3, Bank 4, and Bank 5 for I/O selected to be differential		100		Ω
SE Input Termination	Input Single Ended Termination Resistance	Bank 3, Bank 4, and Bank 5 for I/O selected to be Single Ended	36	40	64	Ω
			46	50	80	
			56	60	96	
			71	75	120	

3.12. sysI/O Differential DC Electrical Characteristics

3.12.1. LVDS

LVDS input buffer on CrossLink-NX is operating with V_{CCAUX} = 1.8 V and independent of Bank V_{CCIO} voltage. LVDS output buffer is powered by the Bank V_{CCIO} at 1.8 V.

LVDS can only be supported in Bank 3, Bank 4, and Bank 5. LVDS25 output can be emulated with LVDS25E in Bank 0, Bank 1, Bank 2, Bank 6, and Bank 7. This is described in LVDS25E (Output Only) section.

Table 3.17. LVDS DC Electrical Characteristics (Over Recommended Operating Conditions)[1]

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{INP}, V_{INM}	Input Voltage	—	0	—	1.60	V
V_{ICM}	Input Common Mode Voltage	Half the sum of the two Inputs	0.05	—	1.55 [2]	V
V_{THD}	Differential Input Threshold	Difference between the two Inputs	±100	—	—	mV
I_{IN}	Input Current	Power On or Power Off	—	—	±10	µA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100 Ω	—	1.425	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100 Ω	0.9 V	1.075	—	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100 Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low	—	—	—	50	mV
V_{OCM}	Output Common Mode Voltage	(V_{OP} + V_{OM})/2, R_T = 100 Ω	1.125	1.25	1.375	V
ΔV_{OCM}	Change in V_{OCM}, $V_{OCM(MAX)}$ - $V_{OCM(MIN)}$	—	—	—	50	mV
I_{SAB}	Output Short Circuit Current	V_{OD} = 0 V Driver outputs shorted to each other	—	—	12	mA
ΔV_{OS}	Change in V_{OS} between H and L	—	—	—	50	mV

Note:

1. LVDS input or output are supported in Bank 3, Bank 4, and Bank 5. LVDS input uses V_{CCAUX} on the differential input comparator, and can be located in any V_{CCIO} voltage bank. LVDS output uses V_{CCIO} on the differential output driver, and can only be located in bank with V_{CCIO} = 1.8 V.
2. V_{ICM} is depending on VID, input differential voltage, so the voltage on pin cannot exceed $V_{INP/INN(min/max)}$ requirements. $V_{ICM(min)}$ = $V_{INP/INN(min)}$ + ½ V_{ID}, $V_{ICM(max)}$ = $V_{INP/INN(max)}$ – ½ V_{ID}. Values in the table is based on minimum V_{ID} of +/- 100 mV.

3.12.2. LVDS25E (Output Only)

Three sides of the CrossLink-NX devices, Top, Left and Right, support LVDS25 outputs with emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3.2 is one possible solution for point-to-point signals.

Table 3.18. LVDS25E DC Conditions

Parameter	Description	Typical	Unit
V_{CCIO}	Output Driver Supply (±5%)	2.50	V
Z_{OUT}	Driver Impedance	20	Ω
R_S	Driver Series Resistor (±1%)	158	Ω
R_P	Driver Parallel Resistor (±1%)	140	Ω
R_T	Receiver Termination (±1%)	100	Ω
V_{OH}	Output High Voltage	1.43	V
V_{OL}	Output Low Voltage	1.07	V
V_{OD}	Output Differential Voltage	0.35	V
V_{CM}	Output Common Mode Voltage	1.25	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	6.03	mA

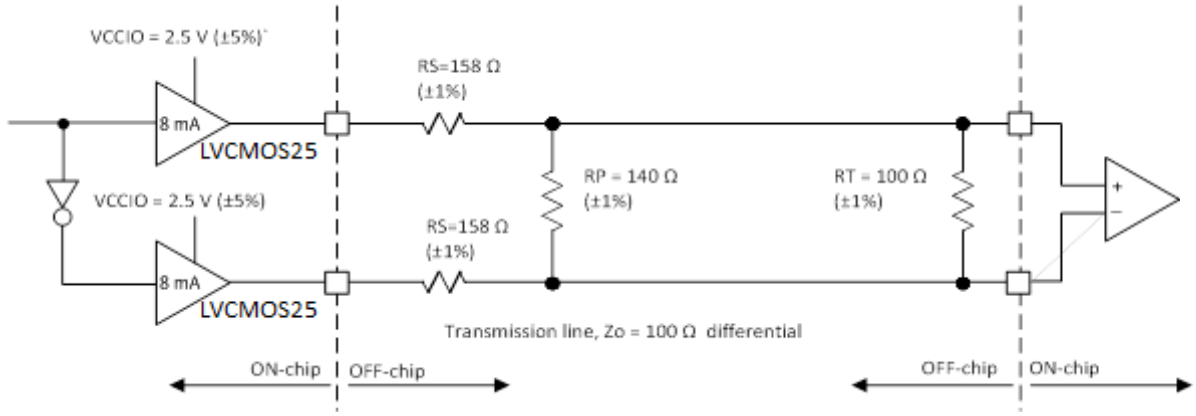


Figure 3.2. LVDS25E Output Termination Example

3.12.3. SubLVDS (Input Only)

SubLVDS is a reduced-voltage form of LVDS signaling, very similar to LVDS. It is a standard used in many camera types of applications, and follow the SMIA 1.0, Part 2: CCP2 Specification. Being similar to LVDS, the CrossLink-NX devices can support the subLVDS input signaling with the same LVDS input buffer. The output for subLVDS is implemented in subLVDSE/subLVDSEH with a pair of LVCMOS18 output drivers (see SubLVDSE/SubLVDSEH (Output Only) section).

Table 3.19. SubLVDS Input DC Electrical Characteristics (Over Recommended Operating Conditions)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{ID}	Input Differential Threshold Voltage	Over V_{ICM} range	70	150	200	mV
V_{ICM}	Input Common Mode Voltage	Half the sum of the two Inputs	0.4	0.9	1.4	V

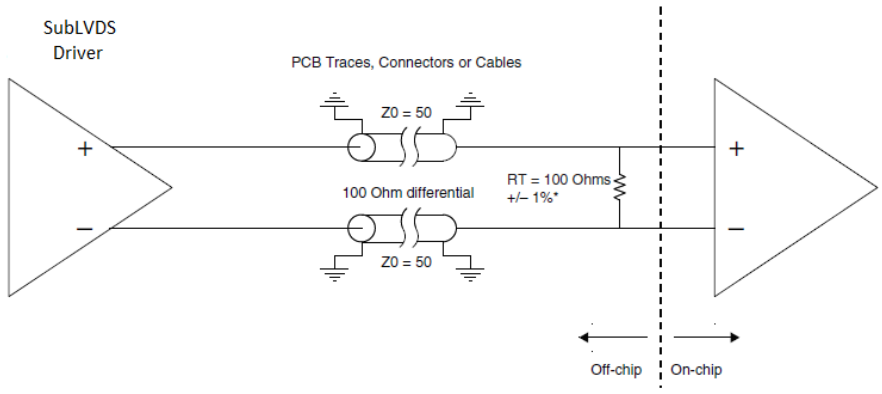


Figure 3.3. SubLVDS Input Interface

3.12.4. SubLVDSE/SubLVDSEH (Output Only)

SubLVDS output uses a pair of LVCMOS18 drivers with True and Complement outputs. The VCCIO of the bank used for subLVDSE or subLVDSEH needs to be powered by 1.8V. SubLVDSE is for Bank 0, Bank 1, Bank 2, Bank 5, and Bank 6; and subLVDSEH is for Bank 3, Bank 4, and Bank 5.

Performance of the subLVDSE/subLVDSEH driver is limited to the performance of LVCMOS18.

Table 3.20. SubLVDS Output DC Electrical Characteristics (Over Recommended Operating Conditions)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{OD}	Output Differential Voltage Swing	—	—	150	—	mV
V_{OCM}	Output Common Mode Voltage	Half the sum of the two Outputs	—	0.9	—	V

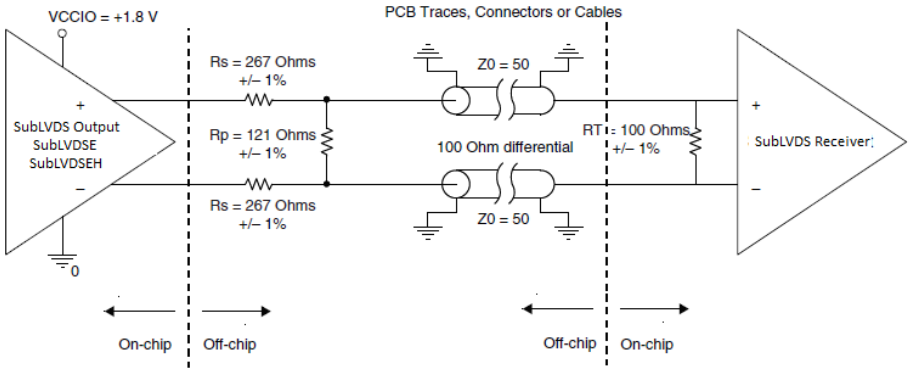


Figure 3.4. SubLVDS Output Interface

3.12.5. SLVS

Scalable Low-Voltage Signaling (SLVS) is based on a point-to-point signaling method defined in the JEDEC JESD8-13 (SLVS-400) standard. This standard evolved from the traditional LVDS standard with smaller voltage swings and a lower common-mode voltage. The 200 mV (400 mV p-p) SLVS swing contributes to a reduction in power.

The CrossLink-NX devices receive SLVS differential input with the LVDS input buffer. This LVDS input buffer is design to cover wide input common mode range that can meet the SLVS input standard specified by the JEDEC standard.

Table 3.21. SLVS Input DC Characteristics (Over Recommended Operating Conditions)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{ID}	Input Differential Threshold Voltage	Over V_{ICM} range	70	—	—	mV
V_{ICM}	Input Common Mode Voltage	Half the sum of the two Inputs	70	200	330	mV

The SLVS output on CrossLink-NX is supported with the LVDS drivers found in Bank 3, Bank 4, and Bank 5. The LVDS driver on CrossLink-NX is a current controlled driver. It can be configured as LVDS driver, or configured with the 100 Ω differential termination with center-tap set to V_{OCM} at 200 mV. This means the differential output driver can be placed into bank with V_{CCIO} = 1.2 V, 1.5 V, or 1.8 V, even if it is powered by V_{CCIO}.

Table 3.22. SLVS Output DC Characteristics (Over Recommended Operating Conditions)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{CCIO}	Bank V_{CCIO}	—	–5%	1.2, 1.5, 1.8	+ 5%	V
V_{OD}	Output Differential Voltage Swing	—	140	200	270	mV
V_{OCM}	Output Common Mode Voltage	Half the sum of the two Outputs	150	200	250	mV
Z_{OS}	Single-Ended Output Impedance	—	37.5	50	62.5	Ω

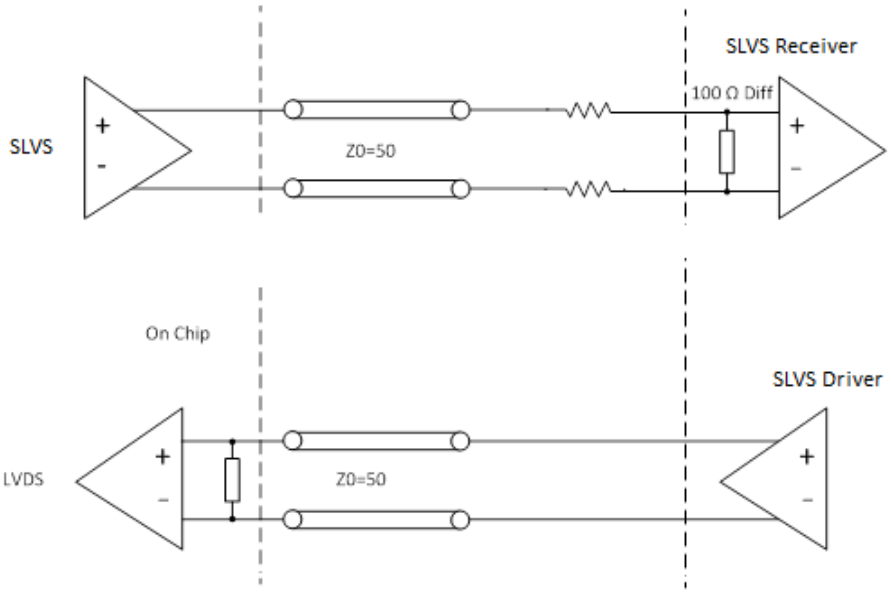


Figure 3.5. SLVS Interface

3.12.6. Soft MIPI D-PHY

When Soft D-PHY is implemented inside the FPGA logic, the I/O interface needs to use sysI/O buffers to connect to external D-PHY pins.

The CrossLink-NX sysI/O provides support of SLVS, as described in SLVS section, plus the LVCMOS12 input / output buffers together to support the High Speed (HS) and Low Power (LP) mode as defined in MIPI Alliance Specification for D-PHY.

To support MIPI D-PHY with SLVS (LVDS) and LVCMOS12, the bank V_{CCIO} cannot be set to 1.5 V or 1.8 V. It has to connect to 1.2 V, or 1.1 V.

All other DC parameters are the same as listed in SLVS section. DC parameters for the LP driver and receiver are the same as listed in LVCMOS12.

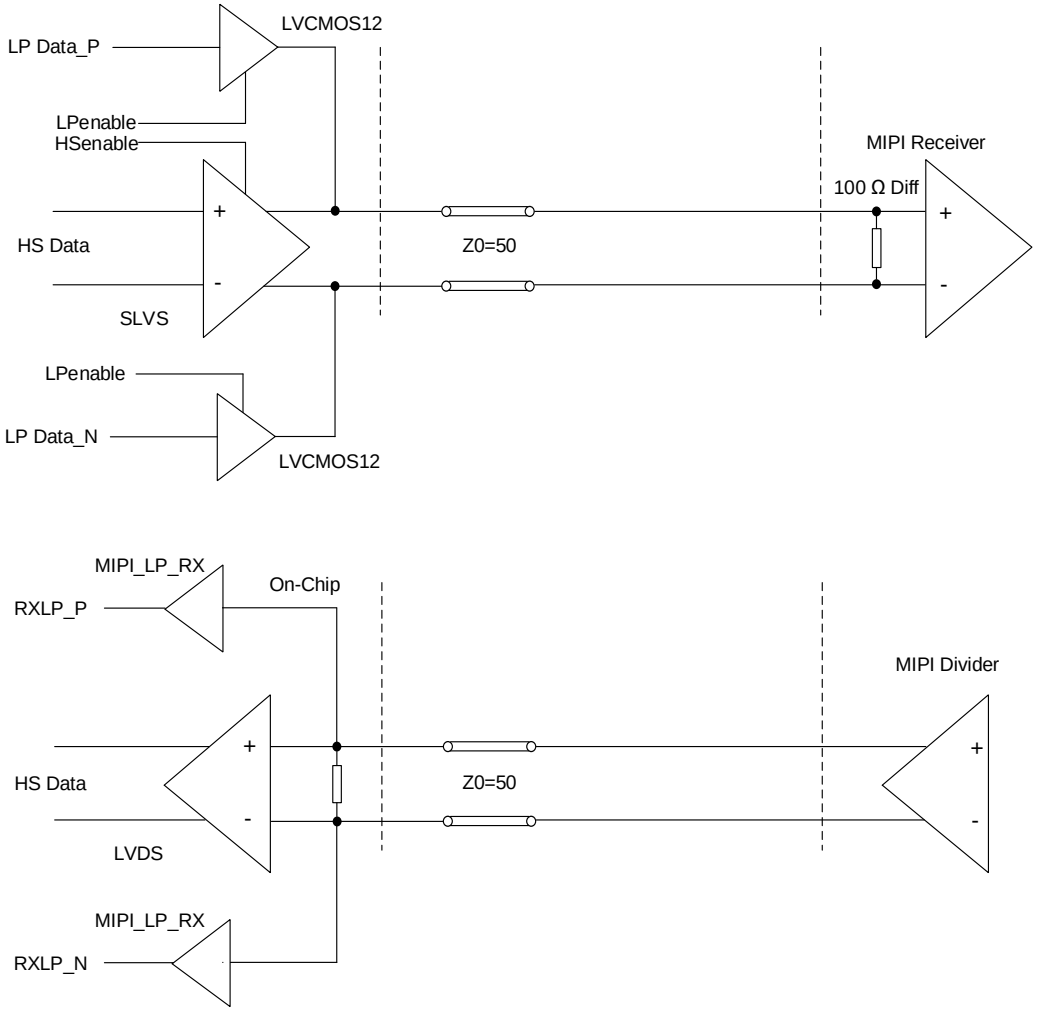


Figure 3.6. MIPI Interface

Table 3.23. Soft D-PHY Input Timing and Levels

Symbol	Description	Conditions	Min	Typ	Max	Unit
High Speed (Differential) Input DC Specifications						
$V_{CMRX(DC)}$	Common-mode Voltage in High Speed Mode	—	70	—	330	mV
V_{IDTH}	Differential Input HIGH Threshold	—	70	—	—	mV
V_{IDTL}	Differential Input LOW Threshold	—	—	—	-70	mV
V_{IHHS}	Input HIGH Voltage (for HS mode)	—	—	—	460	mV
V_{ILHS}	Input LOW Voltage	—	–40	—	—	mV
$V_{TERM-EN}$	Single-ended voltage for HS Termination Enable[4]	—	—	—	450	mV
Z_{ID}	Differential Input Impedance	—	80	100	125	Ω
High Speed (Differential) Input AC Specifications						
$\Delta V_{CMRX(HF)}$[1]	Common-mode Interference (>450 MHz)	—	—	—	100	mV
$\Delta V_{CMRX(LF)}$[2, 3]	Common-mode Interference (50 MHz - 450 MHz)	—	–50	—	50	mV
C_{CM}	Common-mode Termination	—			60	pF
Low Power (Single-Ended) Input DC Specifications						
V_{IH}	Low Power Mode Input HIGH Voltage	—	740	—	—	mV
V_{IL}	Low Power Mode Input LOW Voltage	—	—	—	480	mV
V_{IL-ULP}	Ultra Low Power Input LOW Voltage	—	—	—	300	mV
V_{HYST}	Low Power Mode Input Hysteresis	—	25	—	—	mV
e_{SPIKE}	Input Pulse Rejection	—	—	—	300	V·ps
T_{MIN-RX}	Minimum Pulse Width Response	—	20	—	—	ns
V_{INT}	Peak Interference Amplitude	—	—	—	200	mV
f_{INT}	Interference Frequency	—	450	—	—	MHz

Notes:

1. This is peak amplitude of sine wave modulated to the receiver inputs.
2. Input common-mode voltage difference compared to average common-mode voltage on the receiver inputs.
3. Exclude any static ground shift of 50 mV.
4. High Speed Differential R_{TERM} is enabled when both D_P and D_N are below this voltage.

Table 3.24. Soft D-PHY Output Timing and Levels

Symbol	Description	Conditions	Min	Typ	Max	Unit
High Speed (Differential) Output DC Specifications						
V_{CMTX}	Common-mode Voltage in High Speed Mode	—	150	200	250	mV
$\|\Delta V_{CMTX(1,0)}\|$	V_{CMTX} Mismatch Between Differential HIGH and LOW	—	—	—	5	mV
$\|V_{OD}\|$	Output Differential Voltage	|D-PHY-P – D-PHY-N|	140	200	270	mV
$\|\Delta V_{OD}\|$	V_{OD} Mismatch Between Differential HIGH and LOW	—	—	—	10	mV
V_{OHHS}	Single-Ended Output HIGH Voltage	—	—	—	360	mV
Z_{OS}	Single Ended Output Impedance	—	37.5	50	62.5	Ω
ΔZ_{OS}	Z_{OS} mismatch	—	—	—	20	%
High Speed (Differential) Output AC Specifications						
$\Delta V_{CMTX(LF)}$	Common-Mode Variation, 50 MHz – 450 MHz	—	—	—	25	mV_{RMS}
$\Delta V_{CMTX(HF)}$	Common-Mode Variation, above 450 MHz	—	—	—	15	mV_{RMS}
t_R	Output 20% - 80% Rise Time Output 80% - 20% Fall Time	0.08 Gbps ≤ t_R ≤ 1.00 Gbps	—	—	0.30	UI
		1.00 Gbps < t_R ≤ 1.50 Gbps	—	—	0.35	UI
t_F	Output Data Valid After CLK Output	0.08 Gbps ≤ t_F ≤ 1.00 Gbps	—	—	0.30	UI
		1.00 Gbps < t_F ≤ 1.50 Gbps	—	—	0.35	UI
Low Power (Single-Ended) Output DC Specifications						
V_{OH}	Low Power Mode Output HIGH Voltage	0.08 Gbps – 1.5 Gbps	1.07	1.2	1.3	V
V_{OL}	Low Power Mode Input LOW Voltage	—	–50	—	50	mV
Z_{OLP}	Output Impedance in Low Power Mode	—	110	—	—	Ω
Low Power (Single-Ended) Output AC Specifications						
t_{RLP}	15% - 85% Rise Time	—	—	—	25	ns
t_{FLP}	85% - 15% Fise Time	—	—	—	25	ns
t_{REOT}	HS – LP Mode Rise and Fall Time, 30% - 85%	—	—	—	35	ns
$T_{LP-PULSE-TX}$	Pulse Width of the LP Exclusive-OR Clock	1st LP XOR Clock Pulse after STOP State or Last Pulse before STOP State	40	—	—	ns
		All Other Pulses	20	—	—	ns
$T_{LP-PER-TX}$	Period of the LP Exclusive-OR Clock	—	90	—	—	ns
C_{LOAD}	Load Capacitance	—	0	—	70	pF

Table 3.25. Soft D-PHY Clock Signal Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
Clock Signal Specification						
UI Instantaneous	UI_{INST}	—	—	—	12.5	ns
UI Variation	ΔUI	—	–10%	—	10%	UI
		—	–5%	—	5%	UI

Table 3.26. Soft D-PHY Data-Clock Timing Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
Data-Clock Timing Specifications						
$T_{SKEW[TX]}$	Data to Clock Skew	0.08 Gbps ≤ $T_{SKEW[TX]}$ ≤ 1.00 Gbps	-0.15	—	0.15	UI_{INST}
		1.00 Gbps < $T_{SKEW[TX]}$ ≤ 1.50 Gbps	-0.20	—	0.20	UI_{INST}
$T_{SKEW[TLIS]}$	Data to Clock Skew	0.08 Gbps ≤ $T_{SKEW[TLIS]}$ ≤ 1.00 Gbps	-0.20	—	0.20	UI_{INST}
		1.00 Gbps < $T_{SKEW[TLIS]}$ ≤ 1.50 Gbps	-0.10	—	0.10	UI_{INST}
$T_{SETUP[RX]}$	Input Data Setup Before CLK	0.08 Gbps ≤ $T_{SETUP[RX]}$ ≤ 1.00 Gbps	0.15	—	—	UI
		1.00 Gbps < $T_{SETUP[RX]}$ ≤ 1.50 Gbps	0.20	—	—	UI
$T_{HOLD[RX]}$	Input Data Hold After CLK	0.08 Gbps ≤ $T_{HOLD[RX]}$ ≤ 1.00 Gbps	0.15	—	—	UI
		1.00 Gbps < $T_{HOLD[RX]}$ ≤ 1.50 Gbps	0.20	—	—	UI

3.12.7. Differential HSTL15D (Output Only)

Differential HSTL outputs are implemented as a pair of complementary single-ended HSTL outputs.

3.12.8. Differential SSTL135D, SSTL15D (Output Only)

Differential SSTL is used for differential clock in DDR3/DDR3L memory interface. All differential SSTL outputs are implemented as a pair of complementary single-ended SSTL outputs. All allowable single-ended output classes (class I and class II) are supported.

3.12.9. Differential HSUL12D (Output Only)

Differential HSUL is used for differential clock in LPDDR2/LPDDR3 memory interface. All differential HSUL outputs are implemented as a pair of complementary single-ended HSUL12 outputs. All allowable single-ended drive strengths are supported.

3.12.10. Differential LVCMOS25D, LVCMOS33D, LVTTL33D (Output Only)

Differential LVCMOS and LVTTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output drive strengths are supported.

3.13. CrossLink-NX Maximum sysI/O Buffer Speed

Over recommended operating conditions.

Table 3.27. CrossLink-NX Maximum I/O Buffer Speed[1, 2, 3, 4, 7]

Buffer	Description	Banks	Max	Unit
Maximum sysI/O Input Frequency				
Single-Ended				
LVCMOS33	LVCMOS33, V_{CCIO} = 3.3 V	0, 1, 2, 6, 7	200	MHz
LVTTL33	LVTTL33, V_{CCIO} = 3.3 V	0, 1, 2, 6, 7	200	MHz
LVCMOS25	LVCMOS25, V_{CCIO} = 2.5 V	0, 1, 2, 6, 7	200	MHz
LVCMOS18 [5]	LVCMOS18, V_{CCIO} = 1.8 V	0, 1, 2, 6, 7	200	MHz
LVCMOS18H	LVCMOS18, V_{CCIO} = 1.8 V	3, 4, 5	200	MHz
LVCMOS15 [5]	LVCMOS15, V_{CCIO} = 1.5 V	0, 1, 2, 6, 7	100	MHz
LVCMOS15H [5]	LVCMOS15, V_{CCIO} = 1.5 V	3, 4, 5	150	MHz
LVCMOS12 [5]	LVCMOS12, V_{CCIO} = 1.2 V	0, 1, 2, 6, 7	50	MHz
LVCMOS12H [5]	LVCMOS12, V_{CCIO} = 1.2 V	3, 4, 5	100	MHz
LVCMOS10 [5]	LVCMOS 1.0, V_{CCIO} = 1.2 V	0, 1, 2, 6, 7	50	MHz
LVCMOS10H [5]	LVCMOS 1.0, V_{CCIO} = 1.0 V	3, 4, 5	50	MHz
LVCMOS10R	LVCMOS 1.0, V_{CCIO} independent	3, 4, 5	50	MHz
SSTL15_I, SSTL15_II	SSTL_15, V_{CCIO} = 1.5 V	3, 4, 5	1066	Mbps
SSTL135_I, SSTL135_II	SSTL_135, V_{CCIO} = 1.35 V	3, 4, 5	1066	Mbps
HSUL12	HSUL_12, V_{CCIO} = 1.2 V	3, 4, 5	1066	Mbps
HSTL15	HSTL15, V_{CCIO} = 1.5 V	3, 4, 5	250	Mbps
MIPI D-PHY (LP Mode)	MIPI, Low Power Mode, V_{CCIO} = 1.2 V	3, 4, 5	10	Mbps
Differential				
LVDS	LVDS, V_{CCIO} independent QFN72, caBGA256, csBGA289, and caBGA400	3, 4, 5	1250	Mbps
	LVDS, V_{CCIO} independent csfBGA121	3, 4, 5	1500	Mbps
subLVDS	subLVDS, V_{CCIO} independent QFN72, caBGA256, csBGA289, and caBGA400	3, 4, 5	1250	Mbps
	subLVDS, V_{CCIO} independent csfBGA121	3, 4, 5	1500	Mbps
SLVS	SLVS similar to MIPI HS, V_{CCIO} independent QFN72, caBGA256, csBGA289, caBGA400	3, 4, 5	1250	Mbps
	SLVS similar to MIPI HS, V_{CCIO} independent csfBGA121	3, 4, 5	1500	Mbps
MIPI D-PHY (HS Mode)	MIPI, High Speed Mode, V_{CCIO} = 1.2 V QFN72, caBGA256, csBGA289, caBGA400	3, 4, 5	1250	Mbps
	MIPI, High Speed Mode, V_{CCIO} = 1.2 V csfBGA121	3, 4, 5	1500[8]	Mbps
SSTL15D	Differential SSTL15, V_{CCIO} independent	3, 4, 5	1066	Mbps
SSTL135D	Differential SSTL135, V_{CCIO} independent	3, 4, 5	1066	Mbps
HUSL12D	Differential HSUL12, V_{CCIO} independent	3, 4, 5	1066	Mbps
HSTL15D	Differential HSTL15, V_{CCIO} independent	3, 4, 5	250	Mbps

Buffer	Description	Banks	Max	Unit
Maximum sysI/O Output Frequency				
Single-Ended				
LVCMOS33 (all drive strengths)	LVCMOS33, V_{CCIO} = 3.3 V	0, 1, 2, 6, 7	200	MHz
LVCMOS33 (RS50)	LVCMOS33, V_{CCIO} = 3.3 V, R_{SERIES} = 50 Ω	0, 1, 2, 6, 7	200	MHz
LVTTL33 (all drive strengths)	LVTTL33, V_{CCIO} = 3.3 V	0, 1, 2, 6, 7	200	MHz
LVTTL33 (RS50)	LVTTL33, V_{CCIO} = 3.3 V, R_{SERIES} = 50 Ω	0, 1, 2, 6, 7	200	MHz
LVCMOS25 (all drive strengths)	LVCMOS25, V_{CCIO} = 2.5 V	0, 1, 2, 6, 7	200	MHz
LVCMOS25 (RS50)	LVCMOS25, V_{CCIO} = 2.5 V, R_{SERIES} = 50 Ω	0, 1, 2, 6, 7	200	MHz
LVCMOS18 (all drive strengths)	LVCMOS18, V_{CCIO} = 1.8 V	0, 1, 2, 6, 7	200	MHz
LVCMOS18 (RS50)	LVCMOS18, V_{CCIO} = 1.8 V, R_{SERIES} = 50 Ω	0, 1, 2, 6, 7	200	MHz
LVCMOS18H (all drive strengths)	LVCMOS18, V_{CCIO} = 1.8 V	3, 4, 5	200	MHz
LVCMOS18H (RS50)	LVCMOS18, V_{CCIO} = 1.8 V, R_{SERIES} = 50 Ω	3, 4, 5	200	MHz
LVCMOS15 (all drive strengths)	LVCMOS15, V_{CCIO} = 1.5 V	0, 1, 2, 6, 7	100	MHz
LVCMOS15H (all drive strengths)	LVCMOS15, V_{CCIO} = 1.5 V	3, 4, 5	150	MHz
LVCMOS12 (all drive strengths)	LVCMOS12, V_{CCIO} = 1.2 V	0, 1, 2, 6, 7	50	MHz
LVCMOS12H (all drive strengths)	LVCMOS12, V_{CCIO} = 1.2 V	3, 4, 5	100	MHz
LVCMOS10H (all drive strengths)	LVCMOS12, V_{CCIO} = 1.2 V	3, 4, 5	50	MHz
SSTL15_I, SSTL15_II	SSTL_15, V_{CCIO} = 1.5 V	3, 4, 5	1066	Mbps
SSTL135_I, SSTL135_II	SSTL_135, V_{CCIO} = 1.35 V	3, 4, 5	1066	Mbps
HSUL12 (all drive strengths)	HSUL_12, V_{CCIO} = 1.2 V	3, 4, 5	1066	Mbps
HSTL15	HSTL15, V_{CCIO} = 1.5 V	3, 4, 5	250	Mbps
MIPI D-PHY (LP Mode)	MIPI, Low Power Mode, V_{CCIO} = 1.2 V	3, 4, 5	10	Mbps
Differential[9]				
LVDS	LVDS, V_{CCIO} = 1.8 V QFN72, caBGA256, csBGA289, and caBGA400	3, 4, 5	1250	Mbps
	LVDS, V_{CCIO} = 1.8 V csfBGA121	3, 4, 5	1500	Mbps
LVDS25E[6]	LVDS25, Emulated, V_{CCIO} = 2.5 V	0, 1, 2, 6, 7	400	Mbps
SubLVDSE[6]	subLVDS, Emulated, V_{CCIO} = 1.8 V	0, 1, 2, 6, 7	400	Mbps
SubLVDSEH[6]	subLVDS, Emulated, V_{CCIO} = 1.8 V	3, 4, 5	800	Mbps
SLVS	SLVS similar to MIPI, V_{CCIO} = 1.2 V QFN72, caBGA256, csBGA289, caBGA400	3, 4, 5	1250	Mbps
	SLVS similar to MIPI, V_{CCIO} = 1.2 V csfBGA121	3, 4, 5	1500	Mbps
MIPI D-PHY (HS Mode)	MIPI, High Speed Mode, V_{CCIO} = 1.2 V QFN72, caBGA256, csBGA289, caBGA400	3, 4, 5	1250	Mbps
	MIPI, High Speed Mode, V_{CCIO} = 1.2 V csfBGA121	3, 4, 5	1500[8]	Mbps
SSTL15D	Differential SSTL15, V_{CCIO} = 1.5 V	3, 4, 5	1066	Mbps
SSTL135D	Differential SSTL135, V_{CCIO} = 1.35 V	3, 4, 5	1066	Mbps
HUSL12D	Differential HSUL12, V_{CCIO} = 1.2 V	3, 4, 5	1066	Mbps
HSTL15D	Differential HSTL15, V_{CCIO} = 1.5 V	3, 4, 5	250	Mbps

Notes:

1. Maximum I/O speed is the maximum switching rate of the I/O operating within the guidelines of the defining standard. The actual interface speed performance using the I/O also depends on other factors, such as internal and external timing.
2. These numbers are characterized but not test on every device.

3. Performance is specified in MHz, as defined in clock rate when the sysI/O is used as pin. For data rate performance, this can be converted to Mbps, which equals to 2 times the clock rate.
4. LVCMOS and LVTTL are measured with load specified in Table 3.48.
5. These LVCMOS inputs can be placed in different V_{CCIO} voltage. Performance may vary. Please refer to Lattice Design Software
6. These emulated outputs performance is based on externally properly terminated as described in LVDS25E (Output Only) and SubLVDSE/SubLVDSEH (Output Only).
7. All speeds are measured with fast slew.
8. Subject to verification when package becomes available.
9. For maximum differential I/O performance only Differential I/O should be placed in the bottom I/O banks. If this is not possible, the following impacts on maximum performance:
   a. If Fast Slew Rate LVCMOS I/O are used, they should limited to no more than 9 I/O (adjacent), 4 I/O (same bank), 55 I/O (left/right banks) to keep degradation below 50%.
   b. If non-Differential I/O (SLOW SLEW) are placed on the bottom but not within the same bank as differential I/O, then the maximum Differential performance is degraded to 70% of original when 21 aggressors are toggling.
   c. If non-Differential I/O (SLOW SLEW) are placed within the same bank as Differential I/O then the maximum performance is degraded to 50% of original when 16 aggressor are toggling.
   d. No performance impact if MIPI LP and MIPI HS are in the same bank.
   e. If Differential RX/TX I/O are both placed within the same bank then the maximum performance is degraded to 90%.
   f. For DDR3/3L, LPDDR2/3 separate DQ/DQS groups from Address/Commands/CLK groups into separate banks.

3.14. Typical Building Block Function Performance

These building block functions can be generated using Lattice Design Software Tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.

Table 3.28. Pin-to-Pin Performance

Function	Typ. @ VCC = 1.0 V	Unit
16-Bit Decoder (I/O configured with LVCMOS18, Left and Right Banks)	5.5	ns
16-Bit Decoder (I/O configured with HSTL15_I, Bottom Banks)	5.1	ns
16:1 Mux (I/O configured with LVCMOS18, Left and Right Banks)	6	ns
16:1 Mux (I/O configured with HSTL15_I, Bottom Banks)	6.1	ns

Note: These functions are generated using Lattice Radiant Design Software tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.

Table 3.29. Register-to-Register Performance

Function	Typ. @ VCC = 1.0 V	Unit
Basic Functions		
16-Bit Adder	500[2]	MHz
32-Bit Adder	496	MHz
16-Bit Counter	402	MHz
32-Bit Counter	371	MHz
Embedded Memory Functions		
512 x 36 Single Port RAM, with Output Register	500[2]	MHz
1024 x 18 True-Dual Port RAM using same clock, with EBR Output Registers	500[2]	MHz
1024 x 18 True-Dual Port RAM using asynchronous clocks, with EBR Output Registers	500[2]	MHz
Large Memory Functions		
32K x 32 Single Port RAM, with Output Register	165[2]	MHz
32K x 32 Single Port RAM with ECC, with Output Register	130[2]	MHz
32K x 32 True-Dual Port RAM using same clock, with EBR Output Registers	340	MHz

Function	Typ. @ VCC = 1.0 V	Unit
Distributed Memory Functions		
16 x 4 Single Port RAM (One PFU)	500[2]	MHz
16 x 2 Pseudo-Dual Port RAM (One PFU)	500[2]	MHz
16 x 4 Pseudo-Dual Port (Two PFUs)	500[2]	MHz
DSP Functions		
9 x 9 Multiplier with Input Output Registers	351	MHz
9 x 9 Multiplier with Input/Pipelined/Output Registers	240	MHz
18 x 18 Multiplier with Input/Output Registers	214	MHz
18 x 18 Multiplier with Input/Pipelined/Output Registers	191	MHz
36 x 36 Multiplier with Input/Output Registers	201	MHz
36 x 36 Multiplier with Input/Pipelined/Output Registers	129	MHz
MAC 9 x 9 with Input/Output Registers	218	MHz
MAC 9 x 9 with Input/Pipelined/Output Registers	238	MHz

Notes:
1. The Clock port is configured with LVDS I/O type. Performance Grade: 9_High-Performance_1.0V.
2. Limited by the Minimum Pulse Width of the component
3. These functions are generated using Lattice Radiant Design Software tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.
4. For the Pipelined designs, the number of pipeline stages used are 2.

3.15. LMMI

Table 3.30 summarizes the performance of the LMMI interface with supported IPs. Additional timing requirement and constraint can be identified through the Lattice Radiance design tools.

Table 3.30. LMMI F_{MAX} Summary

IP	F_{MAX} (MHz)
CDR0	73
CDR1	70
DPHY0	67
DPHY1	55
CRE	54
I^2C	38
PCIe	57
PLL_ULC	59
PLL_LLC	55
PLL_LRC	37

3.16. Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Lattice Radiant design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Lattice Radiant design tool can provide logic timing numbers at a particular temperature and voltage.

3.17. CrossLink-NX External Switching Characteristics

Over recommended commercial operating conditions.

Table 3.31. CrossLink-NX External Switching Characteristics (V_{CC} = 1.0 V)

Parameter	Description	–9		–8		–7		Unit
		Min	Max	Min	Max	Min	Max	
Clocks								
Primary Clock								
f_{MAX_PRI}	Frequency for Primary Clock	—	400	—	325.2	—	276	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	1.125	—	1.384	—	1.63	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	—	450	—	554	—	653	ps
Edge Clock								
f_{MAX_EDGE}	Frequency for Edge Clock Tree	—	800	—	650.4	—	551.7	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	0.537	—	0.661	—	0.779	—	ns
t_{SKEW_EDGE}	Edge Clock Skew Within a Device	—	120	—	148	—	174	ps
Generic SDR Input								
General I/O Pin Parameters Using Dedicated Primary Clock Input without PLL								
t_{CO}	Clock to Output - PIO Output Register	—	6.45	—	6.64	—	7.83	ns
t_{SU}	Clock to Data Setup - PIO Input Register	0	—	0	—	0	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	2.94	—	3.32	—	3.92	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	1.84	—	1.84	—	1.84	—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Data Input Delay	0.16	—	0.16	—	0.16	—	ns
General I/O Pin Parameters Using Dedicated Primary Clock Input with PLL								
t_{COPLL}	Clock to Output - PIO Output Register	—	4.02	—	4.67	—	5.51	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	1.23	—	1.23	—	1.23	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	0.98	—	1.21	—	1.42	—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	4.74	—	4.74	—	4.74	—	ns
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Data Input Delay	0	—	0	—	0	—	ns
Generic DDR Input/Output								
Generic DDRX1 Inputs/Outputs with Clock and Data Centered at Pin (GDDRX1_RX/TX.SCLK.Centered) using PCLK Clock Input - Figure 3.7 and Figure 3.9								
t_{SU_GDDR1}	Input Data Setup Before CLK	0.550	—	0.550	—	0.648	—	ns
		0.275	—	0.275	—	0.275	—	UI
t_{HO_GDDR1}	Input Data Hold After CLK	0.550	—	0.550	—	0.648	—	ns

Parameter	Description	–9		–8		–7		Unit
		Min	Max	Min	Max	Min	Max	
t_{DVB_GDDR1}	Output Data Valid After CLK Output	0.700	—	0.631	—	0.744	—	ns
		–0.300	—	–0.369	—	–0.435	—	ns + 1/2 UI
t_{DQVA_GDDR1}	Output Data Valid After CLK Output	0.700	—	0.631	—	0.744	—	ns
		–0.300	—	–0.369	—	–0.435	—	ns + 1/2 UI
f_{DATA_GDDRX1}	Input/Output Data Rate	—	500	—	500.0	—	424	Mbps
f_{MAX_GDDRX1}	Frequency of PCLK	—	250	—	250	—	212	MHz
½ UI	Half of Data Bit Time, or 90 degree	—	—	1.000	—	1.179	—	ns
Output TX to Input RX Margin per Edge		0.150	—	0.081	—	0.095	—	ns
Generic DDRX1 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX1_RX/TX.SCLK.Aligned) using PCLK Clock Input - Figure 3.8 and Figure 3.10								
t_{DVA_GDDR1}	Input Data Valid After CLK	—	-0.550	—	–0.550	—	-0.648	ns + 1/2 UI
		—	0.450	—	0.450	—	0.530	ns
		—	0.225	—	0.225	—	0.225	UI
t_{DVE_GDDR1}	Input Data Hold After CLK	0.550	—	0.550	—	0.648	—	ns + 1/2 UI
		1.550	—	1.550	—	1.827	—	ns
		0.775	—	0.775	—	0.775	—	UI
t_{DIA_GDDR1}	Output Data Invalid After CLK Output	—	0.300	—	0.369	—	0.435	ns
t_{DIB_GDDR1}	Output Data Invalid Before CLK Output	—	0.300	—	0.369	—	0.435	ns
f_{DATA_GDDRX1}	Input/Output Data Rate	—	500	—	500	—	424	Mbps
f_{MAX_GDDRX1}	Frequency for PCLK	—	250	—	250	—	212	MHz
½ UI	Half of Data Bit Time, or 90 degree	1.000	—	1.000	—	1.179	—	ns
Output TX to Input RX Margin per Edge		0.150	—	0.081	—	0.095	—	ns
Generic DDRX2 Inputs/Outputs with Clock and Data Centered at Pin (GDDRX2_RX/TX.ECLK.Centered) using PCLK Clock Input - Figure 3.7 and Figure 3.9								
t_{SU_GDDRX2}	Data Setup before CLK Input	0.175	—	0.175	—	0.206	—	ns
		0.175	—	0.175	—	0.175	—	UI
t_{HO_GDDRX2}	Data Hold after CLK Input	0.177	—	0.177	—	0.206	—	ns
t_{DVB_GDDRX2}	Output Data Valid Before CLK Output	0.380	—	0.352	—	0.415	—	ns
		-0.120	—	–0.148	—	–0.174	—	ns + 1/2 UI
t_{DQVA_GDDRX2}	Output Data Valid After CLK Output	0.380	—	0.352	—	0.415	—	ns
		-0.120	—	–0.148	—	–0.174	—	ns + 1/2 UI
f_{DATA_GDDRX2}	Input/Output Data Rate	—	1000	—	1000	—	848	Mbps
f_{MAX_GDDRX2}	Frequency for ECLK	—	500	—	500	—	424	MHz
½ UI	Half of Data Bit Time, or 90 degree	0.500	—	0.500	—	0.589	—	ns
f_{PCLK}	PCLK frequency	—	250.0	—	250.0	—	212.1	MHz
Output TX to Input RX Margin per Edge		0.230	—	0.202	—	0.239	—	ns
Generic DDRX2 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX2_RX/TX.ECLK.Aligned) using PCLK Clock Input - Figure 3.8 and Figure 3.10								
t_{DVA_GDDRX2}	Input Data Valid After CLK	—	–0.275	—	-0.275	—	–0.324	ns + 1/2 UI
		—	0.225	—	0.225	—	0.265	ns
		—	0.225	—	0.225	—	0.225	UI

Parameter	Description	–9		–8		–7		Unit
		Min	Max	Min	Max	Min	Max	
t_{DVE_GDDRX2}	Input Data Hold After CLK	0.275	—	0.275	—	0.324	—	ns + 1/2 UI
		0.775	—	0.775	—	0.914	—	ns
		0.775	—	0.775	—	0.775	—	UI
t_{DIA_GDDRX2}	Output Data Invalid After CLK Output	—	0.120	—	0.148	—	0.174	ns
t_{DIB_GDDRX2}	Output Data Invalid Before CLK Output	—	0.120	—	0.148	—	0.174	ns
f_{DATA_GDDRX2}	Input/Output Data Rate	—	1000	—	1000	—	848	Mbps
f_{MAX_GDDRX2}	Frequency for ECLK	—	500	—	500	—	424	MHz
½ UI	Half of Data Bit Time, or 90 degree	0.500	—	0.500	—	0.589	—	ns
f_{PCLK}	PCLK frequency	—	250.0	—	250.0	—	212.1	MHz
Output TX to Input RX Margin per Edge		0.105	—	0.077	—	0.091	—	ns
Generic DDRX4 Inputs/Outputs with Clock and Data Centered at Pin (GDDRX4_RX/TX.ECLK.Centered) using PCLK Clock Input - Figure 3.7 and Figure 3.9								
t_{SU_GDDRX4}	Input Data Set-Up Before CLK	0.168	—	0.210	—	0.244	—	ns
		0.252	—	0.252	—	0.252	—	UI
t_{HO_GDDRX4}	Input Data Hold After CLK	0.174	—	0.210	—	0.244	—	ns
t_{DVB_GDDRX4}	Output Data Valid Before CLK Output	0.213	—	0.269	—	0.309	—	
		-0.120	—	–0.148	—	–0.174	—	
t_{DQVA_GDDRX4}	Input/Output Data Rate	0.213	—	0.269	—	0.309	—	
		-0.120	—	–0.148	—	–0.174	—	
f_{DATA_GDDRX4}	Frequency for ECLK	—	1500	—	1200	—	1034	Mbps
f_{MAX_GDDRX4}	PCLK frequency	—	750.0	—	600	—	517	MHz
½ UI	Half of Data Bit Time, or 90 degree	0.333	—	0.417	—	0.483	—	ns
f_{PCLK}	Input Data Set-Up Before CLK	—	187.5	—	150.0	—	129.3	MHz
Output TX to Input RX Margin per Edge		0.080	—	0.102	—	0.116	—	ns
Generic DDRX4 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX4_RX/TX.ECLK.Aligned) using PCLK Clock Input, Left and Right sides Only - Figure 3.8 and Figure 3.10								
t_{DVA_GDDRX4}	Input Data Valid After CLK	—	–0.183	—	–0.229	—	–0.266	ns + 1/2 UI
		—	0.150	—	0.188	—	0.218	ns
		—	0.225	—	0.225	—	0.225	UI
t_{DVE_GDDRX4}	Input Data Hold After CLK	0.183	—	0.229	—	0.266	—	ns + 1/2 UI
		0.517	—	0.646	—	0.749	—	ns
		0.775	—	0.775	—	0.775	—	UI
t_{DIA_GDDRX4}	Output Data Invalid After CLK Output	—	0.120	—	0.148	—	0.17	ns
t_{DIB_GDDRX4}	Output Data Invalid Before CLK Output	—	0.120	—	0.148	—	0.174	ns
f_{DATA_GDDRX4}	Input/Output Data Rate	—	1500	—	1200	—	1034	Mbps
f_{MAX_GDDRX4}	Frequency for ECLK	—	750	—	600	—	517	MHz
½ UI	Half of Data Bit Time, or 90 degree	0.333	—	0.417	—	0.483	—	ns
f_{PCLK}	PCLK frequency	—	187.5	—	150.0	—	129.3	MHz
Output TX to Input RX Margin per Edge		0.030	—	0.040	—	0.044	—	ns

Parameter	Description	–9		–8		–7		Unit
		Min	Max	Min	Max	Min	Max	
Generic DDRX5 Inputs/Outputs with Clock and Data Centered at Pin (GDDRX5_RX/TX.ECLK.Centered) using PCLK Clock Input - Figure 3.7 and Figure 3.9								
t_{SU_GDDRX5}	Input Data Set-Up Before CLK	0.179	—	0.187	—	0.224	—	ns
		0.224	—	0.224	—	0.224	—	UI
t_{HO_GDDRX5}	Input Data Hold After CLK	0.181	—	0.187	—	0.224	—	ns
$t_{WINDOW\_GDDRX5C}$	Input Data Valid Window	0.36	—	0.374	—	0.448	—	ns
t_{DVB_GDDRX5}	Output Data Valid Before CLK Output	0.280	—	0.269	—	0.326	—	ns
		–0.120	—	–0.148	—	–0.174	—	ns+1/2UI
t_{DQVA_GDDRX5}	Output Data Valid After CLK Output	0.280	—	0.269	—	0.326	—	ns
		–0.120	—	–0.148	—	–0.174	—	ns+1/2UI
f_{DATA_GDDRX5}	Input/Output Data Rate	—	1250	—	1200	—	1000	Mbps
f_{MAX_GDDRX5}	Frequency for ECLK	—	625	—	600	—	500	MHz
½ UI	Half of Data Bit Time, or 90 degree	0.400	—	0.417	—	0.500	—	ns
f_{PCLK}	PCLK frequency	—	125.0	—	120.0	—	100.0	MHz
Output TX to Input RX Margin per Edge		0.120	—	0.102	—	0.126	—	ns
Generic DDRX5 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX5_RX/TX.ECLK.Aligned) using PCLK Clock Input - Figure 3.8 and Figure 3.10								
t_{DVA_GDDRX5}	Input Data Valid After CLK	—	–0.220	—	–0.229	—	–0.275	ns + 1/2 UI
		—	0.180	—	0.188	—	0.225	ns
		—	0.225	—	0.225	—	0.225	UI
t_{DVE_GDDRX5}	Input Data Hold After CLK	0.220	—	0.229	—	0.275	—	ns + 1/2 UI
		0.620	—	0.646	—	0.775	—	ns
		0.775	—	0.775	—	0.775	—	UI
$t_{WINDOW\_GDDRX5A}$	Input Data Valid Window	0.440	—	0.458	—	0.550	—	ns
t_{DIA_GDDRX5}	Output Data Invalid After CLK Output	—	0.120	—	0.148	—	0.174	ns
t_{DIB_GDDRX5}	Output Data Invalid Before CLK Output	—	0.120	—	0.148	—	0.174	ns
f_{DATA_GDDRX5}	Input/Output Data Rate	—	1250	—	1200	—	1000	Mbps
f_{MAX_GDDRX5}	Frequency for ECLK	—	625	—	600	—	500	MHz
½ UI	Half of Data Bit Time, or 90 degree	0.400	—	0.417	—	0.500	—	ns
f_{PCLK}	PCLK frequency	—	125.0	—	120.0	—	100.0	MHz
Output TX to Input RX Margin per Edge		0.060	—	0.040	—	0.051	—	ns
Soft D-PHY DDRX4 Inputs/Outputs with Clock and Data Centered at Pin, using PCLK Clock Input								
$t_{SU\_GDDRX4\_MP}$	Input Data Set-Up Before CLK	0.133	—	0.167	—	0.193	—	ns
		0.2	—	0.2	—	0.2	—	UI
$t_{HO\_GDDRX4\_MP}$	Input Data Hold After CLK	0.133	—	0.167	—	0.193	—	ns
$t_{DVB\_GDDRX4\_MP}$	Output Data Valid Before CLK Output	0.133	—	0.167	—	0.193	—	ns
		0.2	—	0.2	—	0.2	—	UI
$t_{DQVA\_GDDRX4\_MP}$	Output Data Valid After CLK Output	0.133	—	0.167	—	0.193	—	ns
		0.2	—	0.2	—	0.2	—	UI
$f_{DATA\_GDDRX4\_MP}$	Input Data Bit Rate for MIPI PHY	—	1500	—	1200	—	1034	Mbps
½ UI	Half of Data Bit Time, or 90 degree	0.333	—	0.417	—	0.483	—	ns
f_{PCLK}	PCLK frequency	—	187.5	—	150.0	—	129.3	MHz

Parameter	Description	–9		–8		–7		Unit
		Min	Max	Min	Max	Min	Max	
Output TX to Input RX Margin per Edge		0.067		0.083		0.097		ns
Video DDRX71 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX71_RX.ECLK) using PLL Clock Input - Figure 3.12 and Figure 3.13								
t_{RPBi_DVA}	Input Valid Bit "i" switch from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	0.264	—	0.264	—	0.3	UI
		—	–0.250	—	–0.250	—	–0.249	ns+(1/2+i)*UI
t_{RPBi_DVE}	Input Hold Bit "i" switch from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	0.722	—	0.722	—	0.7	—	UI
		0.235	—	0.235	—	0.249	—	ns+(1/2+i)*UI
t_{TPBi_DOV}	Data Output Valid Bit "i" switch from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	0.159	—	0.159	—	0.187	ns+i*UI
t_{TPBi_DOI}	Data Output Invalid Bit "i" switch from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	-0.159	—	-0.159	—	-0.187	—	ns+(i+ 1)*UI
$t_{TPBi\_skew\_UI}$	TX skew in UI	—	0.150	—	0.150	—	0.150	UI
t_B	Serial Data Bit Time, = 1UI	1.058	—	1.058	—	1.247	—	ns
f_{DATA_TX71}	DDR71 Serial Data Rate	—	945	—	945	—	802	Mbps
f_{MAX_TX71}	DDR71 ECLK Frequency	—	473	—	473	—	401	MHz
f_{CLKIN}	7:1 Clock (PCLK) Frequency	—	135.0	—	135.0	—	114.5	MHz
Output TX to Input RX Margin per Edge		0.159	—	0.159	—	0.187	—	ns
Memory Interface								
DDR3/DDR3L/LPDDR2/LPDDR3 READ (DQ Input Data are Aligned to DQS) - Figure 3.8								
t_{DVBDQ_DDR3} t_{DVBDQ_DDR3L} t_{DVBDQ_LPDDR2} t_{DVBDQ_LPDDR3}	Data Input Valid before DQS Input	—	–0.235	—	–0.235	—	–0.277	ns + 1/2 UI
t_{DVADQ_DDR3} t_{DVADQ_DDR3L} t_{DVADQ_LPDDR2} t_{DVADQ_LPDDR3}	Data Input Valid after DQS Input	0.235	—	0.235	—	0.277	—	ns + 1/2 UI
f_{DATA_DDR3} f_{DATA_DDR3L} f_{DATA_LPDDR2} f_{DATA_LPDDR3}	DDR Memory Data Rate	—	1066	—	1066	—	904	Mb/s
$f_{MAX\_ECLK\_DDR3}$ $f_{MAX\_ECLK\_DDR3L}$ $f_{MAX\_ECLK\_LPDDR2}$ $f_{MAX\_ECLK\_LPDDR3}$	DDR Memory ECLK Frequency	—	533	—	533	—	452	MHz
$f_{MAX\_SCLK\_DDR3}$ $f_{MAX\_SCLK\_DDR3L}$ $f_{MAX\_SCLK\_LPDDR2}$ $f_{MAX\_SCLK\_LPDDR3}$	DDR Memory SCLK Frequency	—	133.3	—	133.3	—	113	MHz
DDR3/DDR3L/LPDDR2/LPDDR3 WRITE (DQ Output Data are Centered to DQS) - Figure 3.11								
t_{DQVBS_DDR3} t_{DQVBS_DDR3L} t_{DQVBS_LPDDR2} t_{DQVBS_LPDDR3}	Data Output Valid before DQS Output	—	–0.235	—	–0.235	—	–0.277	ns + 1/2 UI
t_{DQVAS_DDR3} t_{DQVAS_DDR3L} t_{DQVAS_LPDDR2} t_{DQVAS_LPDDR3}	Data Output Valid after DQS Output	0.235	—	0.235	—	0.277	—	ns + 1/2 UI

Parameter	Description	–9		–8		–7		Unit
		Min	Max	Min	Max	Min	Max	
f_{DATA_DDR3} f_{DATA_DDR3L} f_{DATA_LPDDR2} f_{DATA_LPDDR3}	DDR Memory Data Rate	—	1066	—	1066	—	904	Mb/s
$f_{MAX\_ECLK\_DDR3}$ $f_{MAX\_ECLK\_DDR3L}$ $f_{MAX\_ECLK\_LPDDR2}$ $f_{MAX\_ECLK\_LPDDR3}$	DDR Memory ECLK Frequency	—	533	—	533	—	452	MHz
$f_{MAX\_SCLK\_DDR3}$ $f_{MAX\_SCLK\_DDR3L}$ $f_{MAX\_SCLK\_LPDDR2}$ $f_{MAX\_SCLK\_LPDDR3}$	DDR Memory SCLK Frequency	—	133.3	—	133.3	—	113	MHz

Notes:

1. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Lattice Radiant software.
2. General I/O timing numbers are based on LVCMOS 1.8, 8 mA, Fast Slew Rate, 0 pf load.
   Generic DDR timing are numbers based on LVDS I/O.
   DDR3 timing numbers are based on SSTL15.
   LPDDR2 and LPDDR3 timing numbers are based on HSUL12.
3. Uses LVDS I/O standard for measurements.
4. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
5. All numbers are generated with the Lattice Radiant software.

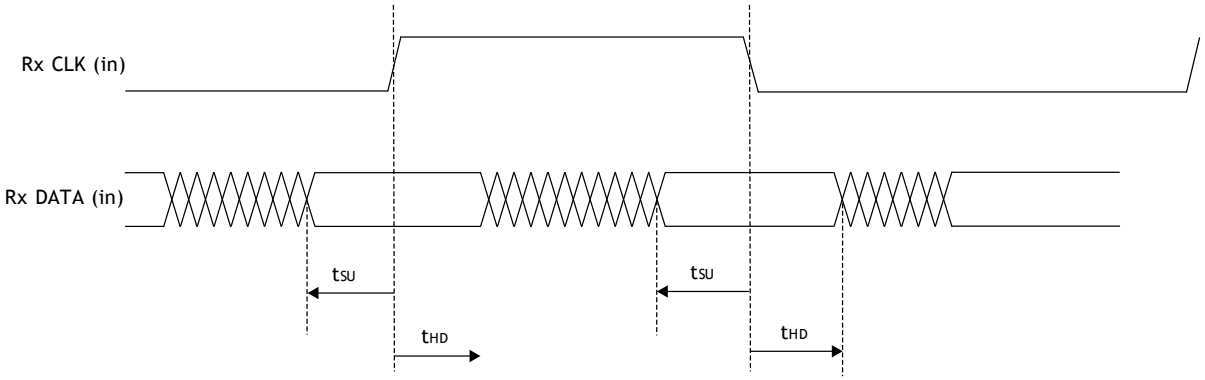


Figure 3.7. Receiver RX.CLK.Centered Waveforms

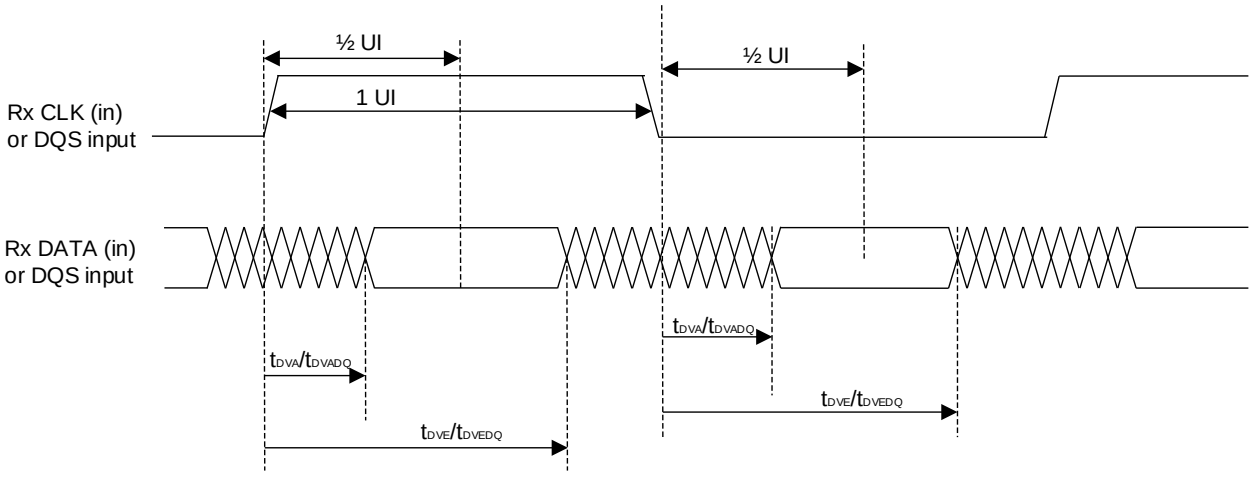


Figure 3.8. Receiver RX.CLK.Aligned and DDR Memory Input Waveforms

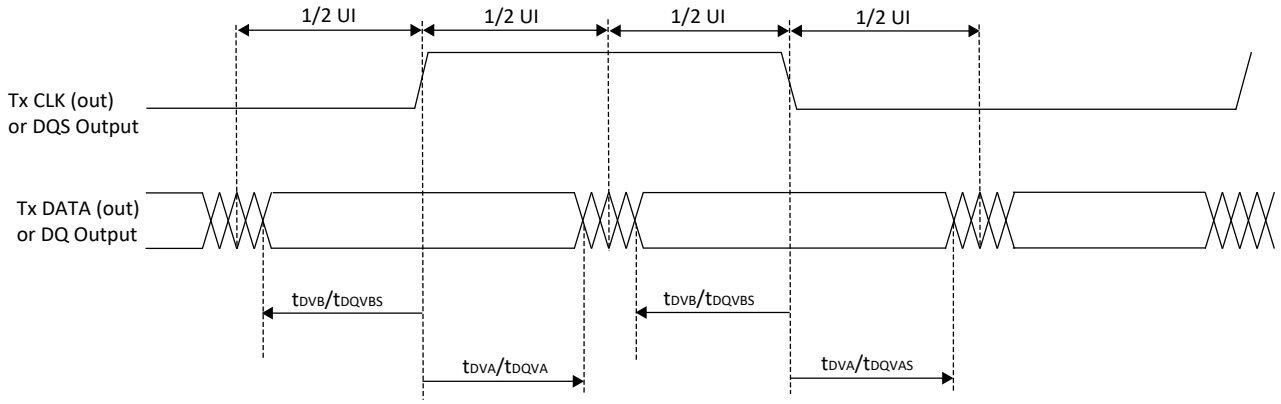


Figure 3.9. Transmit TX.CLK.Centered and DDR Memory Output Waveforms

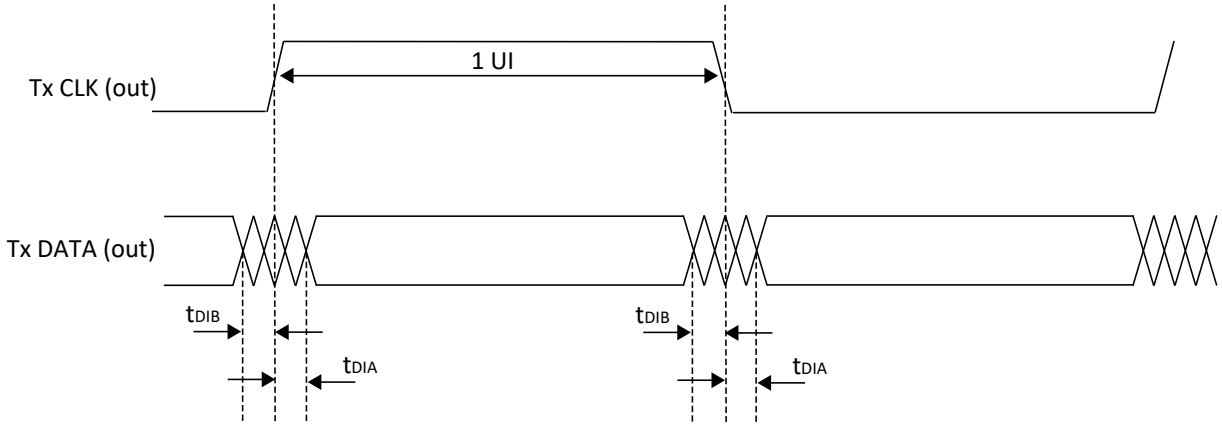
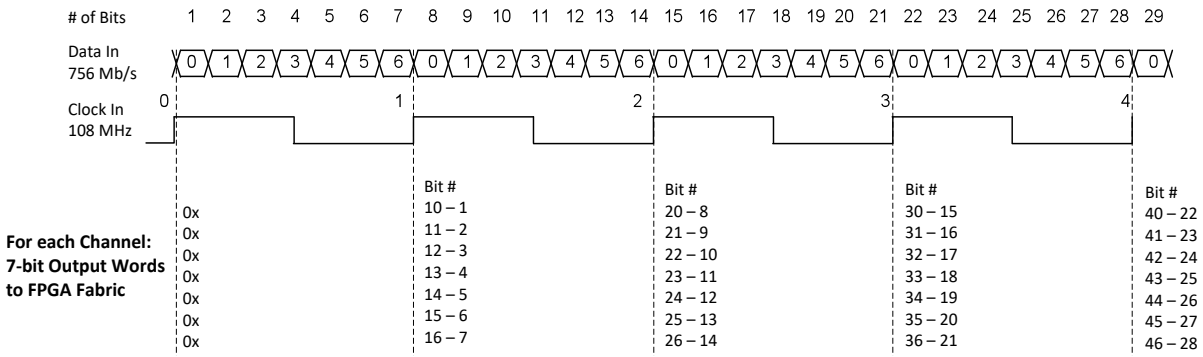


Figure 3.10. Transmit TX.CLK.Aligned Waveforms

Receiver – Shown for one LVDS Channel



Transmitter – Shown for one LVDS Channel

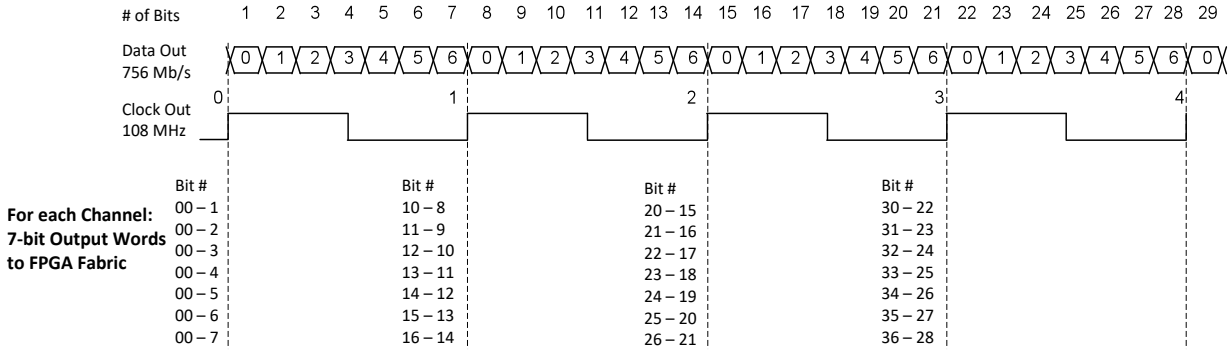


Figure 3.11. DDRX71 Video Timing Waveforms

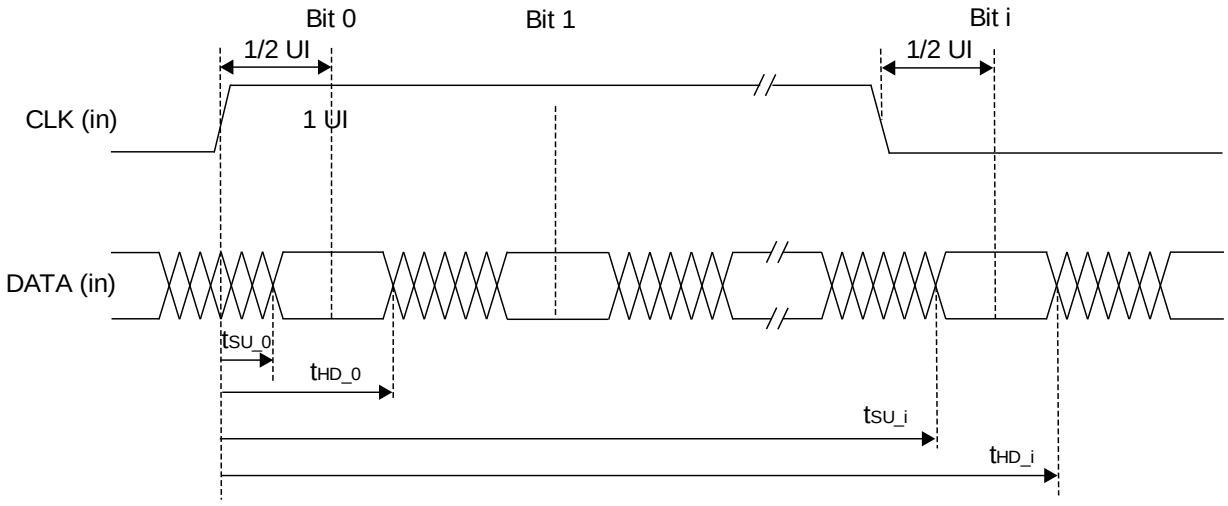


Figure 3.12. Receiver DDRX71_RX Waveforms

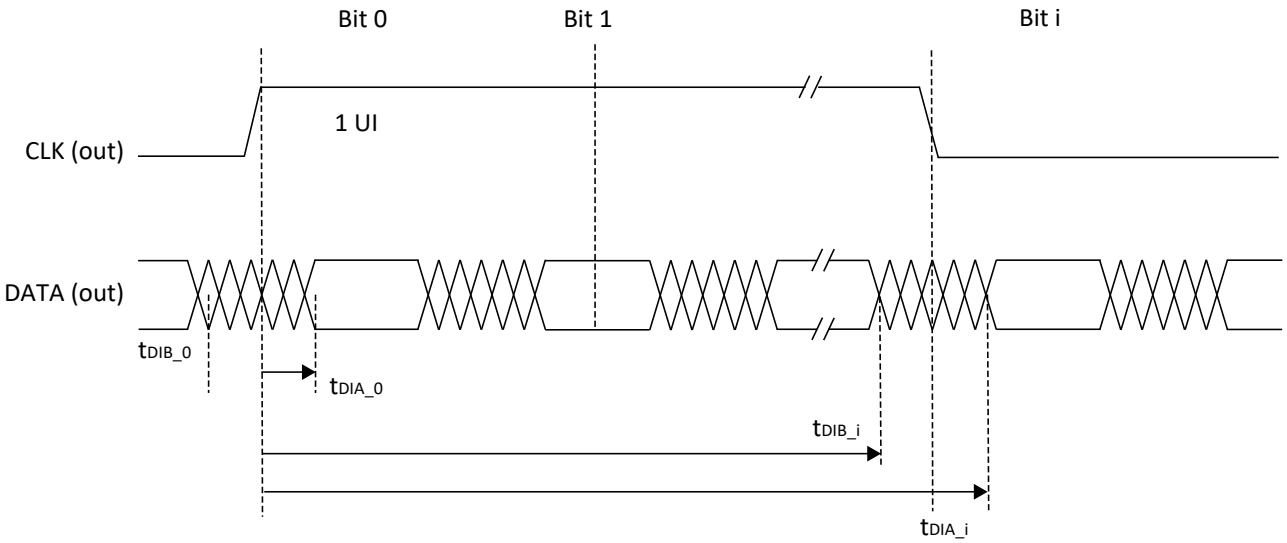


Figure 3.13. Transmitter DDRX71_TX Waveforms

3.18. CrossLink-NX sysCLOCK PLL Timing (V_{CC} = 1.0 V)

Over recommended operating conditions.

Table 3.32. sysCLOCK PLL Timing (V_{CC} = 1.0 V)

Parameter	Descriptions	Conditions	Min	Typ.	Max	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		10	—	500	MHz
f_{OUT}	Output Clock Frequency		6.25	—	800	MHz
f_{VCO}	PLL VCO Frequency		800	—	1600	MHz
f_{PFD}[3]	Phase Detector Input Frequency	Without Fractional-N Enabled	10	—	500	MHz
		With Fractional-N Enabled	10	—	100	MHz
AC Characteristics						
t_{DT}	Output Clock Duty Cycle		45	—	55	%
t_{PH4}	Output Phase Accuracy		–5	—	5	%
t_{OPJIT}[1]	Output Clock Period Jitter	$f_{OUT} \geq 200$ MHz	—	—	250	ps p-p
		$f_{OUT} < 200$ MHz	—	—	0.05	UIPP
	Output Clock Cycle-to-Cycle Jitter	$f_{OUT} \geq 200$ MHz	—	—	250	ps p-p
		$f_{OUT} < 200$ MHz	—	—	0.05	UIPP
	Output Clock Phase Jitter	$f_{PFD} \geq 200$ MHz	—	—	350	ps p-p
		$f_{PFD} < 200$ MHz	—	—	0.05	UIPP
	Output Clock Period Jitter (Fractional-N)	$f_{OUT} \geq 200$ MHz	—	—	350	ps p-p
		$f_{OUT} < 200$ MHz	—	—	0.07	UIPP
	Output Clock Cycle-to-Cycle Jitter (Fractional-N)	$f_{OUT} \geq 200$ MHz	—	—	400	ps p-p
		$f_{OUT} < 200$ MHz	—	—	0.08	UIPP
f_{BW}[4]	PLL Loop Bandwidth		0.45		13	MHz
t_{LOCK}[2]	PLL Lock-in Time		—	—	10	ms
t_{UNLOCK}	PLL Unlock Time (from RESET goes HIGH)		—	—	50	ns
t_{IPJIT}	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	—	500	ps p-p
		$f_{PFD} < 20$ MHz	—	—	0.01	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	—	ns
t_{RST}	RST/ Pulse Width		1	—	—	ms

Notes:

1. Jitter sample is taken over 10,000 samples for Period jitter, and 1,000 samples for Cycle-to-Cycle jitter of the primary PLL output with clean reference clock with no additional I/O toggling.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for $f_{PFD} > 10$ MHz. For $f_{PFD} < 10$ MHz, the jitter numbers may not be met in certain conditions.
4. Result from Lattice Radiant software.

3.19. CrossLink-NX Internal Oscillators Characteristics

Table 3.33. Internal Oscillators (V_{CC} = 1.0 V)

Symbol	Parameter Description	Min	Typ	Max	Unit
f_{CLKHF}	HFOSC CLKK Clock Frequency	405	450	495	MHz
f_{CLKLF}	LFOSC CLKK Clock Frequency	25.6	32	38.4	kHz
DCH_{CLKHF}	HFOSC Duty Cycle (Clock High Period)	45	50	55	%
DCH_{CLKLF}	LFOSC Duty Cycle (Clock High Period)	45	50	55	%

3.20. CrossLink-NX User I²C Characteristics

Table 3.34. User I²C Specifications (V_{CC} = 1.0 V)

Symbol	Parameter Description	STD Mode			FAST Mode			FAST Mode Plus[2]			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{scl}	SCL Clock Frequency	—	—	100	—	—	400	—	—	1000	kHz
T_{DELAY}[1]	Optional delay through delay block	—	—	62	—	—	62	—	—	62	ns

Notes:

1. Refer to the I²C Specification for timing requirements. User design should set constraints in Lattice Design Software to meet this industrial I²C Specification.
2. Fast Mode Plus maximum speed may be achieved by using external pull up resistor on I²C bus. Internal pull up may not be sufficient to support the maximum speed.

3.21. CrossLink-NX Analog-Digital Converter (ADC) Block Characteristics

Table 3.35. ADC Specifications

Symbol	Description	Condition	Min	Typ	Max	Unit
V_{REFINT_ADC}	ADC Internal Reference Voltage		1.14	1.2	1.26	V
V_{REFEXT_ADC}	ADC External Reference Voltage		1.0	—	1.8	V
N_{RES_ADC}	ADC Resolution		—	12	—	bits
$ENOB_{ADC}$	Effective Number of Bits		9.97	11	—	bits
V_{SR_ADC}	ADC Input Range	Bipolar Mode, Internal V_{REF}	$V_{CM\_ADC} - V_{REFINT\_ADC/4}$	V_{CM_ADC}	$V_{CM\_ADC} + V_{REFINT\_ADC/4}$	V
		Bipolar Mode, External V_{REF}	$V_{CM\_ADC} - V_{REFEXT\_ADC/4}$	V_{REFEXT_ADC}	$V_{CM\_ADC} + V_{REFEXT\_ADC/4}$	V
		Uni-polar Mode, Internal V_{REF}	0	—	V_{REFINT_ADC}	V
		Uni-polar Mode, External V_{REF}	0	—	V_{REFEXT_ADC}	V
V_{CM_ADC}	ADC Input Common Mode Voltage (for fully differential signals)	Internal V_{REF}	—	$V_{REFINT\_ADC/2}$	—	V
		External V_{REF}	—	$V_{REFEXT\_ADC/2}$	—	V
f_{CLK_ADC}	ADC Clock Frequency		—	25	40	MHz
DC_{CLK_ADC}	ADC Clock Duty Cycle		48	50	52	%
f_{INPUT_ADC}	ADC Input Frequency		—	—	500	kHz
FS_{ADC}	ADC Sampling Rate		—	1	—	MS/s
N_{TRACK_ADC}	ADC Input Tracking Time		2	—	—	cycles

Symbol	Description	Condition	Min	Typ	Max	Unit
R_{IN_ADC}	ADC Input Equivalent Resistance	1 MS/s, Sampled @ 2 clock cycles	—	116	—	KΩ
t_{CAL_ADC}	ADC Calibration Time		—	—	6500	cycles
L_{OUTput_ADC}	ADC Conversion Time		25	—	—	cycles
DNL_{ADC}	ADC Differential Nonlinearity		–1	—	1	LSB
INL_{ADC}	ADC Integral Nonlinearity		–2	—	2	LSB
$SFDR_{ADC}$	ADC Spurious Free Dynamic Range		67.7	77	—	dBc
THD_{ADC}	ADC Total Harmonic Distortion		—	–76	–66.8	dB
SNR_{ADC}	ADC Signal to Noise Ratio	—	62	67.5	—	dB
$SNDR_{ADC}$	ADC Signal to Noise Plus Distortion Ratio	—	61	67	—	dB
ERR_{GAIN_ADC}	ADC Gain Error	—	–0.5	—	0.5	% FS_{ADC}
ERR_{OFFSET_ADC}	ADC Offset Error	—	–2	—	2	LSB
C_{IN_ADC}	ADC Input Equivalent Capacitance	—	—	2	—	pF

3.22. CrossLink-NX Comparator Block Characteristics

Table 3.36. Comparator Specifications

Symbol	Description	Min	Typ	Max	Unit
f_{IN_COMP}	Comparator Input Frequency	—	—	10	MHz
V_{IN_COMP}	Comparator Input Voltage	0	—	$V_{CCADC18}$	V
V_{OFFSET_COMP}	Comparator Input Offset	–23	—	24	mV
V_{HYST_COMP}	Comparator Input Hysteresis	10	—	31	mV
$V_{LATENCY\_COMP}$	Comparator Latency	—	—	31	ns

3.23. CrossLink-NX Digital Temperature Readout Characteristics

Digital temperature Readout (DTR) is implemented in one of the channels of ADC1.

Table 3.37. DTR Specifications

Symbol	Description	Condition	Min	Typ	Max	Unit
DTR_{RANGE}	DTR Detect Temperature Range	—	–40	—	125	˚C
$DTR_{ACCURACY}$	DTR Accuracy	with external voltage reference range of 1.2 V to 1.8 V	–4	—	4	˚C
		with external voltage reference range of 1.0 V to 1.2 V	–8.6	—	8.6	
$DTR_{RESOLUTION}$	DTR Resolution	with external voltage reference	–0.3	—	0.3	˚C

3.24. CrossLink-NX Hardened MIPI D-PHY Characteristics

Table 3.38. Hardened D-PHY Input Timing and Levels

Symbol	Description	Conditions	Min	Typ	Max	Unit
High Speed (Differential) Input DC Specifications						
$V_{CMRX(DC)}$	Common-mode Voltage in High Speed Mode	—	70	—	330	mV
V_{IDTH}	Differential Input HIGH Threshold	0.08 Gbps ≤ V_{IDTH} ≤ 1.5 Gbps	70	—	—	mV
		1.5 Gbps < V_{IDTH} ≤ 2.5 Gbps	70	—	—	mV
V_{IDTL}	Differential Input LOW Threshold	0.08 Gbps ≤ V_{IDTL} ≤ 1.5 Gbps	—	—	–70	mV
		1.5 Gbps < V_{IDTL} ≤ 2.5 Gbps	—	—	–70	mV
V_{IHHS}	Input HIGH Voltage (for HS mode)	—	—	—	460	mV
V_{ILHS}	Input LOW Voltage	—	–40	—	—	mV
$V_{TERM-EN}$	Single-ended voltage for HS Termination Eanble[4]	—	—	—	450	mV
Z_{ID}	Differential Input Impedance	—	80	100	125	Ω
High Speed (Differential) Input AC Specifications						
$\Delta V_{CMRX(HF)}$[1]	Common-mode Interference (>450 MHz)	0.08 Gbps ≤ $\Delta V_{CMRX(HF)}$ ≤ 1.5 Gbps	—	—	100	mV
		1.5 Gbps < $\Delta V_{CMRX(HF)}$ ≤ 2.5 Gbps	—	—	50	mV
$\Delta V_{CMRX(LF)}$[2, 3]	Common-mode Interference (50 MHz - 450 MHz)	0.08 Gbps ≤ $\Delta V_{CMRX(LF)}$ ≤ 1.5 Gbps	–50	—	50	mV
		1.5 Gbps < $\Delta V_{CMRX(LF)}$ ≤ 2.5 Gbps	–25	—	25	mV
C_{CM}	Common-mode Termination	—	—	—	60	pF
Low Power (Single-Ended) Input DC Specifications						
V_{IH}	Low Power Mode Input HIGH Voltage	—	760	—	—	mV
V_{IL}	Low Power Mode Input LOW Voltage	—	—	—	550	mV
V_{IL-ULP}	Ultra Low Power Input LOW Voltage	—	—	—	300	mV
V_{HYST}	Low Power Mode Input Hysteresis	—	25	—	—	mV
e_{SPIKE}	Input Pulse Rejection	—	—	—	300	V·ps
T_{MIN-RX}	Minimum Pulse Width Response	—	20	—	—	ns
V_{INT}	Peak Interference Amplitude	—	—	—	200	mV
f_{INT}	Interference Frequency	—	450	—	—	MHz
Contention Detector (LP-CD) DC Specifications						
V_{IHCD}	Contention Detect HIGH Voltage	—	450	—	—	mV
V_{ILCD}	Contention Detect LOW Voltage	—	—	—	200	mV

Notes:

1. This is peak amplitude of sine wave modulated to the receiver inputs.
2. Input common-mode voltage difference compared to average common-mode voltage on the receiver inputs.
3. Exclude any static ground shift of 50 mV.
4. High Speed Differential R_{TERM} is enabled when both DP and DN are below this voltage.

Table 3.39. Hardened D-PHY Output Timing and Levels

Symbol	Description	Conditions	Min	Typ	Max	Unit
High Speed (Differential) Output DC Specifications						
V_{CMTX}	Common-mode Voltage in High Speed Mode	—	150	200	250	mV
$\|\Delta V_{CMTX(1,0)}\|$	V_{CMTX} Mismatch Between Differential HIGH and LOW	—	—	—	5	mV
$\|V_{OD}\|$	Output Differential Voltage	|D-PHY-P – D-PHY-N|	140	200	270	mV
$\|\Delta V_{OD}\|$	V_{OD} Mismatch Between Differential HIGH and LOW	—	—	—	14	mV
V_{OHHS}	Single-Ended Output HIGH Voltage	—	—	—	360	mV
Z_{OS}	Single Ended Output Impedance	—	40	50	68	Ω
ΔZ_{OS}	Z_{OS} mismatch	—	—	—	20	%
High Speed (Differential) Output AC Specifications						
$\Delta V_{CMTX(LF)}$	Common-Mode Variation, 50 MHz – 450 MHz	—	—	—	25	mV_{RMS}
$\Delta V_{CMTX(HF)}$	Common-Mode Variation, above 450 MHz	—	—	—	15	mV_{RMS}
t_R	Output 20% - 80% Rise Time	0.08 Gbps ≤ t_R ≤ 1 Gbps	—	—	0.30	UI
		1 Gbps < t_R ≤ 1.5 Gbps	—	—	0.35	UI
		t_R ≤ 1.5 Gbps	100	—	—	ps
		1.5 Gbps < t_R ≤ 2.5 Gbps	—	—	0.40	UI
		t_R > 1.5 Gbps	50	—	—	ps
t_F	Output 80% - 20% Fall Time	0.08 Gbps ≤ t_F ≤ 1 Gbps	—	—	0.30	UI
		1 Gbps < t_F ≤ 1.5 Gbps	—	—	0.35	UI
		t_F ≤ 1.5 Gbps	100	—	—	ps
		1.5 Gbps < t_F ≤ 2.5 Gbps	—	—	0.40	UI
		t_F > 1.5 Gbps	50	—	—	ps
Low Power (Single-Ended) Output DC Specifications						
V_{OH}	Low Power Mode Output HIGH Voltage	0.08 Gbps ≤ V_{OH} ≤ 1.50 Gbps	1.1	1.2	1.3	V
		V_{OH} > 1.50 Gbps	0.95	—	1.3	V
V_{OL}	Low Power Mode Input LOW Voltage	—	–50	—	50	mV
Z_{OLP}	Output Impedance in Low Power Mode	—	106	—	—	Ω
Low Power (Single-Ended) Output AC Specifications						
t_{RLP}	15% - 85% Rise Time	—	—	—	25	ns
t_{FLP}	85% - 15% Fise Time	—	—	—	25	ns
t_{REOT}	HS – LP Mode Rise and Fall Time, 30% - 85%	—	—	—	35	ns
$T_{LP-PULSE-TX}$	Pulse Width of the LP Exclusive-OR Clock	1st LP XOR Clock Pulse after STOP State or Last Pulse before STOP State	40	—	—	ns
		All Other Pulses	20	—	—	ns
$T_{LP-PER-TX}$	Period of the LP Exclusive-OR Clock	—	90	—	—	ns
$\delta V/\delta t_{SR}$	Slew Rate @ C_{LOAD} = 0 pF	—	—	—	500	mV/ns
	Slew Rate @ C_{LOAD} = 5 pF	—	—	—	300	mV/ns
	Slew Rate @ C_{LOAD} = 20 pF	—	—	—	250	mV/ns

Symbol	Description	Conditions	Min	Typ	Max	Unit
	Slew Rate @ C_{LOAD} = 70 pF		—	—	150	mV/ns
	Slew Rate @ C_{LOAD} = 0 to 70 pF (Falling Edge Only)		30	—	—	mV/ns
			25	—	—	mV/ns
	Slew Rate @ C_{LOAD} = 0 to 70 pF (Rising Edge Only)		30	—	—	mV/ns
			25	—	—	mV/ns
	Slew Rate @ C_{LOAD} = 0 to 70 pF (Rising Edge Only)		30 - 0.075* ($V_{O,INST}$ - 700)	—	—	mV/ns
			25 - 0.0625* ($V_{O,INST}$ - 550)	—	—	mV/ns
C_{LOAD}	Load Capacitance		0	—	70	pF

Table 3.40. Hardened D-PHY Pin Characteristic Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
Pin Characteristic Specifications						
V_{PIN}	Pin Signal Voltage Range		–50	—	1350	mV
V_{PIN_LVLP}	Pin Signal Voltage Range in LVLP Operation		–50	—	1150	mV
I_{LEAK}	Pin Leakage Current		–100	—	100	µA
V_{GNDSH}	Ground Shift		–50	—	50	mV
$V_{PIN(absmax)}$	Transient Pin Voltage Level		–0.15	—	1.45	V
$T_{VPIN(absmax)}$	Maximum Transient Time above $V_{PIN(max)}$ or below $V_{PIN(min)}$		—	—	20	ns

Table 3.41. Hardened D-PHY Clock Signal Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
Clock Signal Specification						
UI Instantaneous	UI_{INST}	—	—	—	12.5	ns
UI Variation	ΔUI	—	–10%	—	10%	UI
		—	–5%	—	5%	UI

Table 3.42. Hardened D-PHY Data-Clock Timing Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
Data-Clock Timing Specifications						
$T_{SKEW[TX]}$	Data to Clock Skew	0.08 Gbps ≤ $T_{SKEW[TX]}$ ≤ 1.00 Gbps	–0.15	—	0.15	UI_{INST}
		1.00 Gbps < $T_{SKEW[TX]}$ ≤ 1.50 Gbps	–0.20	—	0.20	UI_{INST}
$T_{SETUP[RX]}$	Input Data Setup Before CLK	0.08 Gbps ≤ $T_{SETUP[RX]}$ ≤ 1.00 Gbps	0.15	—	—	UI
		1.00 Gbps < $T_{SETUP[RX]}$ ≤ 1.50 Gbps	0.20	—	—	UI
$T_{HOLD[RX]}$	Input Data Hold After CLK	0.08 Gbps ≤ $T_{HOLD[RX]}$ ≤ 1.00 Gbps	0.15	—	—	UI
		1.00 Gbps < $T_{HOLD[RX]}$ ≤ 1.50 Gbps	0.20	—	—	UI
F_{IN_DPHY}	Input frequency to Hardened D-PHY PLL		24		200	MHz
$T_{SKEW[TX]}$ Dynamic	Dynamic Data to Clock Skew (Tx)	> 1.5 Gbps	–0.15	—	0.15	UI_{INST}
ISI	Channel ISI	> 1.5 Gbps	—	—	0.20	UI_{INST}
$T_{SETUP[RX]}$ + $T_{HOLD[RX]}$ Dynamic	Dynamic Data to Clock Skew Window Rx Tolerance	> 1.5 Gbps	0.50	—	—	UI_{INST}

3.25. CrossLink-NX Hardened PCIe Characteristics

3.25.1. PCIe (2.5 Gb/s)

Over recommended operating conditions.

Table 3.43. PCIe (2.5 Gb/s)

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Transmitter[1]						
UI	Unit Interval	—	399.88	400	400.12	ps
BW_{TX}	Tx PLL bandwidth	—	1.5	—	22	MHz
$V_{TX-DIFF-PP}$	Differential p-p Tx voltage swing	—	0.8	—	1.2	Vp-p
$V_{TX-DIFF-PP-LOW}$	Low power differential p-p Tx voltage swing	—	0.4	—	1.2	Vp-p
$V_{TX-DE-RATIO-3.5dB}$	Tx de-emphasis level ratio at 3.5dB	—	3	—	4	dB
$T_{TX-RISE-FALL}$	Transmitter rise and fall time	—	0.125	—	—	UI
T_{TX-EYE}	Transmitter Eye, including all jitter sources	—	0.75	—	—	UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Max. time between jitter median and max deviation from the median	—	—	—	0.125	UI
$RL_{TX-DIFF}$	Tx Differential Return Loss, including pkg and silicon	—	10	—	—	dB
RL_{TX-CM}	Tx Common Mode Return Loss, including pkg and silicon	50 MHz < freq < 2.5 GHz	6	—	—	dB
$Z_{TX-DIFF-DC}$	DC differential Impedance	—	80	—	120	Ω

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
$V_{TX-CM-AC-P}$	Tx AC peak common mode voltage, RMS	—	—	—	20	mV, RMS
$I_{TX-SHORT}$	Transmitter short-circuit current	—	—	—	90	mA
$V_{TX-DC-CM}$	Transmitter DC common-mode voltage	—	0	—	1.2	V
$V_{TX-IDLE-DIFF-AC-p}$	Electrical Idle Output peak voltage	—	—	—	20	mV
$V_{TX-RCV-DETECT}$	Voltage change allowed during Receiver Detect	—	—	—	600	mV
$T_{TX-IDLE-MIN}$	Min. time in Electrical Idle	—	20	—	—	ns
$T_{TX-IDLE-SET-TO-IDLE}$	Max. time from EI Order Set to valid Electrical Idle	—	—	—	8	ns
$T_{TX-IDLE-TO-DIFF-DATA}$	Max. time from Electrical Idle to valid differential output	—	—	—	8	ns
$L_{TX-SKEW}$	Lane-to-Lane output skew		—	—	500 ps + 2 UI	ps
Receiver[2]						
UI	Unit Interval	—	399.88	400	400.12	ps
$V_{RX-DIFF-PP}$	Differential Rx peak-peak voltage	—	0.175	—	1.2	Vp-p
T_{RX-EYE}[3]	Receiver eye opening time	—	0.4	—	—	UI
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$[3]	Max time delta between median and deviation from median	—	—	—	0.3	UI
$RL_{RX-DIFF}$	Receiver differential Return Loss, package plus silicon	—	10	—	—	dB
RL_{RX-CM}	Receiver common mode Return Loss, package plus silicon	—	6	—	—	dB
Z_{RX-DC}	Receiver DC single ended impedance	—	40	—	60	Ω
$Z_{RX-DIFF-DC}$	Receiver DC differential impedance	—	80	—	120	Ω
$Z_{RX-HIGH-IMP-DC}$	Receiver DC single ended impedance when powered down	—	200K	—	—	Ω
$V_{RX-CM-AC-P}$[3]	Rx AC peak common mode voltage	—		—	150	mV, peak
$V_{RX-IDLE-DET-DIFF-PP}$	Electrical Idle Detect Threshold	—	65	—	175	mVp-p
$L_{RX-SKEW}$	Receiver –lane-lane skew			—	20	ps

Notes:

1. Refer to PCI Express Base Specification Revision 3.0 Table 4.18 test condition and requirement for respective parameters.
2. Refer to PCI Express Base Specification Revision 3.0 Table 4.24 test condition and requirement for respective parameters.
3. Spec compliant requirement

3.25.2. PCIe (5 Gb/s)

Over recommended operating conditions.

Table 3.44. PCIe (5 Gb/s)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Transmit[1]						
UI	Unit Interval	—	199.94	200	200.06	ps
$B_{WTX-PKG-PLL1}$	Tx PLL bandwidth corresponding to $PKG_{TX-PLL1}$	—	8	—	16	MHz
$B_{WTX-PKG-PLL2}$	Tx PLL bandwidth corresponding to $PKG_{TX-PLL2}$	—	5	—	16	MHz
$P_{KGTX-PLL1}$	Tx PLL Peaking corresponding to $PKG_{TX-PLL1}$	—	—	—	3	dB
$P_{KGTX-PLL2}$	Tx PLL Peaking corresponding to $PKG_{TX-PLL2}$	—	—	—	1	dB
$V_{TX-DIFF-PP}$	Differential p-p Tx voltage swing	—	0.8	—	1.2	V, p-p
$V_{TX-DIFF-PP-LOW}$	Low power differential p-p Tx voltage swing	—	0.4	—	1.2	V, p-p
$V_{TX-DE-RATIO-3.5dB}$	Tx de-emphasis level ratio at 3.5dB	—	3	—	4	dB
$V_{TX-DE-RATIO-6dB}$	Tx de-emphasis level ratio at 6dB	—	5.5	—	6.5	dB
$T_{MIN-PULSE}$	Instantaneous lone pulse width	—	0.9	—	—	UI
$T_{TX-RISE-FALL}$	Transmitter rise and fall time	—	0.15	—	—	UI
T_{TX-EYE}	Transmitter Eye, including all jitter sources	—	0.75	—	—	UI
T_{TX-DJ}	Tx deterministic jitter > 1.5 MHz	—	—	—	0.15	UI
T_{TX-RJ}	Tx RMS jitter < 1.5 MHz	—	—	—	3	ps, RMS
$T_{RF-MISMATCH}$	Tx rise/fall time mismatch	—	—	—	0.1	UI
$R_{LTX-DIFF}$	Tx Differential Return Loss, including package and silicon	50 MHz < freq < 1.25 GHz	10	—	—	dB
		1.25 GHz < freq < 2.5 GHz	8	—	—	dB
R_{LTX-CM}	Tx Common Mode Return Loss, including package and silicon	50 MHz < freq < 2.5 GHz	6	—	—	dB
$Z_{TX-DIFF-DC}$	DC differential Impedance	—	—	—	120	Ω
$V_{TX-CM-AC-PP}$	Tx AC peak common mode voltage, peak-peak	—	—	—	150	mV, p-p
$I_{TX-SHORT}$	Transmitter short-circuit current	—	—	—	90	mA
$V_{TX-DC-CM}$	Transmitter DC common-mode voltage	—	0	—	1.2	V
$V_{TX-IDLE-DIFF-DC}$	Electrical Idle Output DC voltage	—	0	—	5	mV
$V_{TX-IDLE-DIFF-AC-p}$	Electrical Idle Differential Output peak voltage	—	—	—	20	mV
$V_{TX-RCV-DETECT}$	Voltage change allowed during Receiver Detect	—	—	—	600	mV
$T_{TX-IDLE-MIN}$	Min. time in Electrical Idle	—	20	—	—	ns
$T_{TX-IDLE-SET-TO-IDLE}$	Max. time from EI Order Set to valid Electrical Idle	—	—	—	8	ns

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
$T_{TX-IDLE-TO-DIFF-DATA}$	Max. time from Electrical Idle to valid differential output	—	—	—	8	ns
Receive[2]						
$L_{TX-SKEW}$	Lane-to-Lane output skew	—	—	—	500 + 4 UI	ps
UI	Unit Interval	—	199.94	200	200.06	ps
$V_{RX-DIFF-PP}$	Differential Rx peak-peak voltage	—	0.34[3]	—	1.2	V, p-p
$T_{RX-RJ-RMS}$	Receiver random jitter tolerance (RMS)	1.5 MHz – 100 MHz Random noise	—	—	4.2	ps, RMS
T_{RX-DJ}	Receiver deterministic jitter tolerance	—	—	—	88	ps
$R_{LRX-DIFF}$	Receiver differential Return Loss, package plus silicon	50 MHz < freq < 1.25 GHz	10	—	—	dB
		1.25 GHz < freq < 2.5 GHz	8	—	—	dB
R_{LRX-CM}	Receiver common mode Return Loss, package plus silicon	—	6	—	—	dB
Z_{RX-DC}	Receiver DC single ended impedance	—	40	—	60	Ω
$Z_{RX-HIGH-IMP-DC}$	Receiver DC single ended impedance when powered down	—	200K	—	—	Ω
$V_{RX-CM-AC-P}$[3]	Rx AC peak common mode voltage	—	—	—	150	mV, peak
$V_{RX-IDLE-DET-DIFF-PP}$	Electrical Idle Detect Threshold	—	65	—	175[3]	mv, pp
$L_{RX-SKEW}$	Receiver –lane-lane skew	—	—	—	8	ns

Notes:
1. Refer to PCI Express Base Specification Revision 3.0 Table 4.18 test condition and requirement for respective parameters.
2. Refer to PCI Express Base Specification Revision 3.0 Table 4.24 test condition and requirement for respective parameters.
3. Spec compliant requirement

3.26. CrossLink-NX Hardened SGMII Receiver Characteristics

3.26.1. SGMII Rx Specifications

Over recommended operating conditions.

Table 3.45. SGMII Rx

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
f_{DATA}	SGMII Data Rate	—	—	1250	—	MHz
f_{REFCLK}	SGMII Reference Clock Frequency (Data Rate / 10)	—	—	125	—	MHz
J_{TOL_Dj}	Jitter Tolerance, Deterministic	Periodic jitter < 100 KHz		—	0.1*	UI
J_{TOL_Tj}	Jitter Tolerance, Total	Periodic jitter < 100 KHz		—	0.3*	UI
Δf/f	Data Rate and Reference Clock Accuracy	—	–300	—	300	ppm

***Note:** J_{TOT} can meet the following jitter mask specification: 0 to 2 KHz: 5 UI; 2 to 500 KHz: log-log slope 5 UI to 0.02 UI; above 500 KHz: 0.02 UI.

3.27. CrossLink-NX sysCONFIG Port Timing Specifications

Over recommended operating conditions.

Table 3.46. CrossLink-NX sysCONFIG Port Timing Specifications

Symbol	Parameter	Device	Min	Typ.	Max	Unit
Master SPI POR / REFRESH Timing						
t_{ICFG}	Time during POR, from V_{CC}, V_{CCAUX}, V_{CCIO0} or V_{CCIO1} (whichever is the last) pass POR trip voltage, or REFRESH command executed, to the rising edge of INITN	—	—	—	30	µs
t_{VMC}	Time from rising edge of INITN to the valid Master MCLK	—	—	—	5	µs
f_{MCLK_DEF}	Default MCLK frequency (Before MCLK frequency selection in bitstream)	—	—	150	—	MHz
Slave SPI/I²C/I3C POR / REFRESH Timing						
t_{MSPI_INH}	Time during POR, from V_{CC}, V_{CCAUX}, V_{CCIO0} or V_{CCIO1} (whichever is the last) pass POR trip voltage, or REFRESH command executed, to pull PROGRAMN LOW to prevent entering MSPI mode	—	—	—	1	µs
$t_{ACT\_PROGRAMN\_H}$	Minimum time driving PROGRAMN HIGH after last activation clock	—	50	—	—	ns
t_{CONFIG_CCLK}	Minimum time to start driving CCLK (SSPI) after PROGRAMN HIGH	—	50	—	—	ns
t_{CONFIG_SCL}	Minimum time to start driving SCL (I²C/I3C) after PROGRAMN HIGH	—	50	—	—	ns
PROGRAMN Configuration Timing						
$t_{PROGRAMN}$	PROGRAMN LOW pulse accepted	—	50	—	—	ns
$t_{PROGRAMN\_RJ}$	PROGRAMN LOW pulse rejected	—	—	—	25	ns
t_{INIT_LOW}	PROGRAMN LOW to INITN LOW	—	—	—	100	ns
t_{INIT_HIGH}	PROGRAMN LOW to INITN HIGH	LIFCL-40	—	30	—	µs
		LIFCL-17	—	30	—	µs
t_{DONE_LOW}	PROGRAMN LOW to DONE LOW	—	—	—	35	µs
t_{DONE_HIGH}	PROGRAMN HIGH to DONE HIGH	—		—	2	s
t_{IODISS}	PROGRAMN LOW to I/O Disabled	—	—	—	125	ns
Master SPI						
f_{MCLK}*	Max selected MCLK output frequency	—	—	150	165	MHz
f_{MCLK_DC}	MCLK output clock duty cycle	—	40	—	60	%
t_{MCLKH}	MCLK output clock pulse width HIGH	—	3	—	—	ns
t_{MCLKL}	MCLK output clock pulse width LOW	—	3	—	—	ns
t_{SU_MSI}	MSI to MCLK setup time	—	3	—	—	ns
t_{HD_MSI}	MSI to MCLK hold time	—	0.5	—	—	ns
t_{CO_MSO}	MCLK to MSO delay	—	—	—	12	ns
Slave SPI						
f_{CCLK}	CCLK input clock frequency	—	—	—	135	MHz
t_{CCLKH}	CCLK input clock pulse width HIGH	—	3.5	—	—	ns
t_{CCLKL}	CCLK input clock pulse width LOW	—	3.5	—	—	ns
t_{VMC_SLAVE}	Time from rising edge of INITN to Slave CCLK driven	—	50	—	—	ns
t_{VMC_MASTER}	CCLK input clock duty cycle	—	40	—	60	%
t_{SU_SSI}	SSI to CCLK setup time	—	3.2	—	—	ns

Symbol	Parameter	Device	Min	Typ.	Max	Unit
t_{HD_SSI}	SSI to CCLK hold time	—	1.9	—	—	ns
t_{CO_SSO}	CCLK falling edge to valid SSO output	—	—	—	16	ns
t_{EN_SSO}	CCLK falling edge to SSO output enabled	—	—	—	16	ns
t_{DIS_SSO}	CCLK falling edge to SSO output disabled	—	—	—	16	ns
t_{HIGH_SCSN}	SCSN HIGH time	—	74	—	—	ns
t_{SU_SCSN}	SCSN to CCLK setup time	—	3.5	—	—	ns
t_{HD_SCSN}	SCSN to CCLK hold time	—	1.6	—	—	ns
I²C/I3C						
f_{SCL_I2C}	SCL input clock frequency for I²C	—	—	—	1	MHz
f_{SCL_I3C}	SCL input clock frequency for I3C	—	—	—	12	MHz
t_{SCLH}	SCL input clock pulse width HIGH	—	400	—	—	ns
t_{SCLL}	SCL input clock pulse width LOW	—	400	—	—	ns
t_{SU_SDA}	SDA to SCL setup time	—	100	—	—	ns
t_{HD_SDA}	SDA to SCL hold time	—	300	—	—	ns
t_{CO_SDA}	SCL falling edge to valid SDA output	—	—	—	30	ns
t_{EN_SDA}	SCL falling edge to SDA output enabled	—	—	—	30	ns
t_{DIS_SDA}	SCL falling edge to SDA output disabled	—	—	—	30	ns
Wake-Up Timing						
t_{DONE_HIGH}	Last configuration clock cycle to DONE going HIGH	—	—	—	60	µs
t_{FIO_EN}	User I/O enabled in Fast I/O Mode	LIFCL-40	—		6.245	M cycles
		LIFCL-17	—		2.321	M cycles
t_{IOEN}	Config clock to user I/O enabled	—	130	—	—	ns
t_{MCLKZ}	Master MCLK to Hi-Z	—	—	—	2.5	µs

*__Note__: f_{MCLK} has a dependency on HFOSC and is 1/3 of f_{CLKHF}.

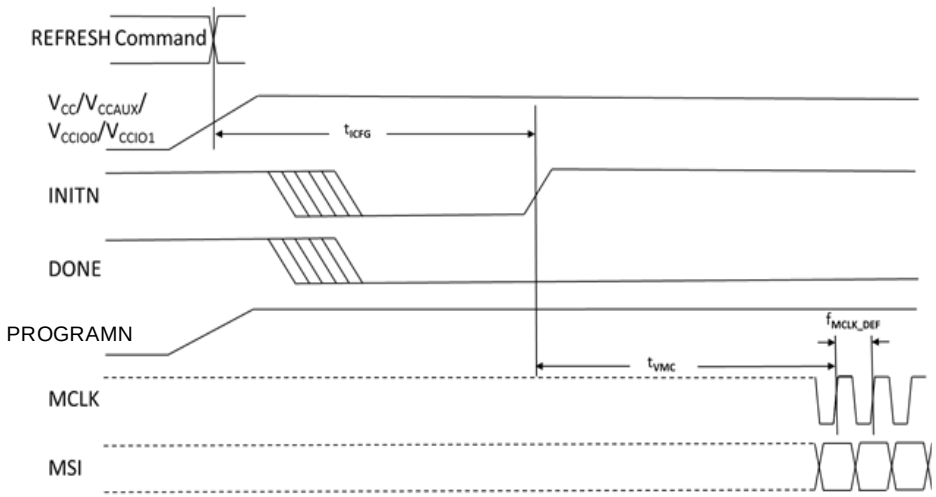


Figure 3.14. Master SPI POR/REFRESH Timing

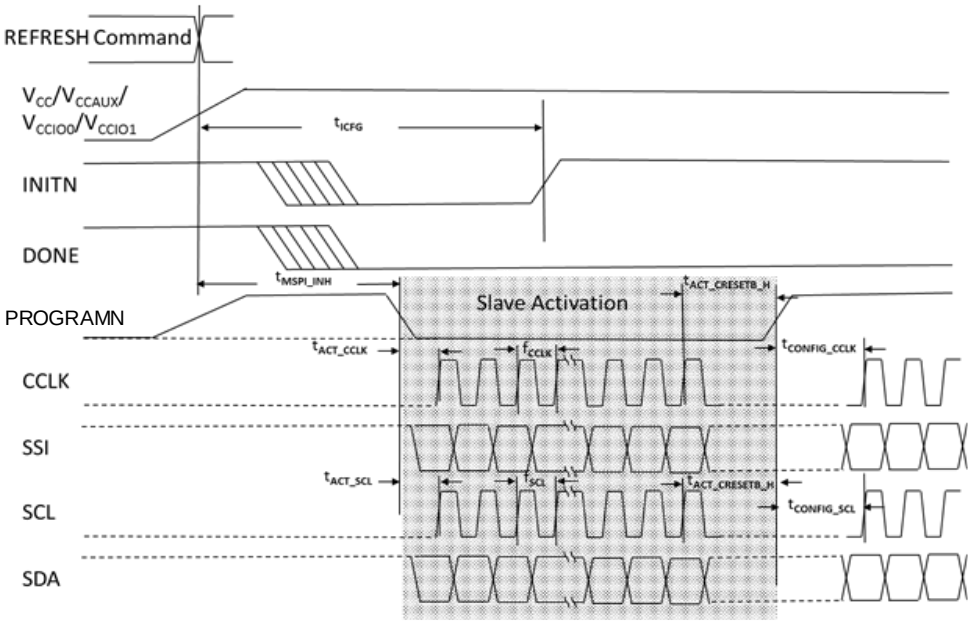


Figure 3.15. Slave SPI/I²C/I3C POR/REFRESH Timing

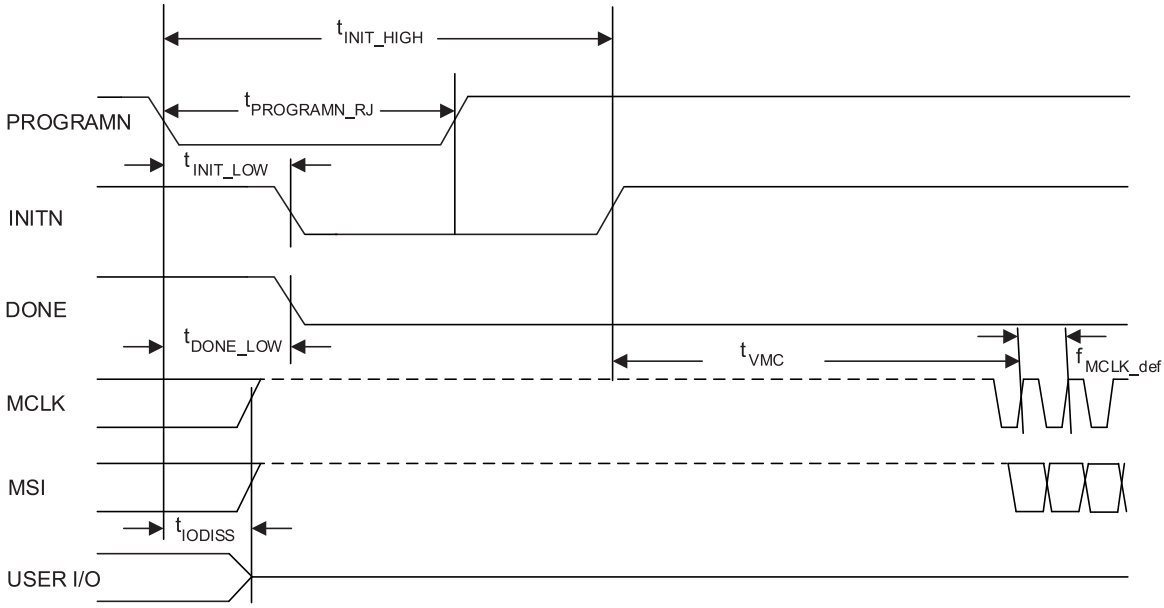


Figure 3.16. Master SPI PROGRAMN Timing

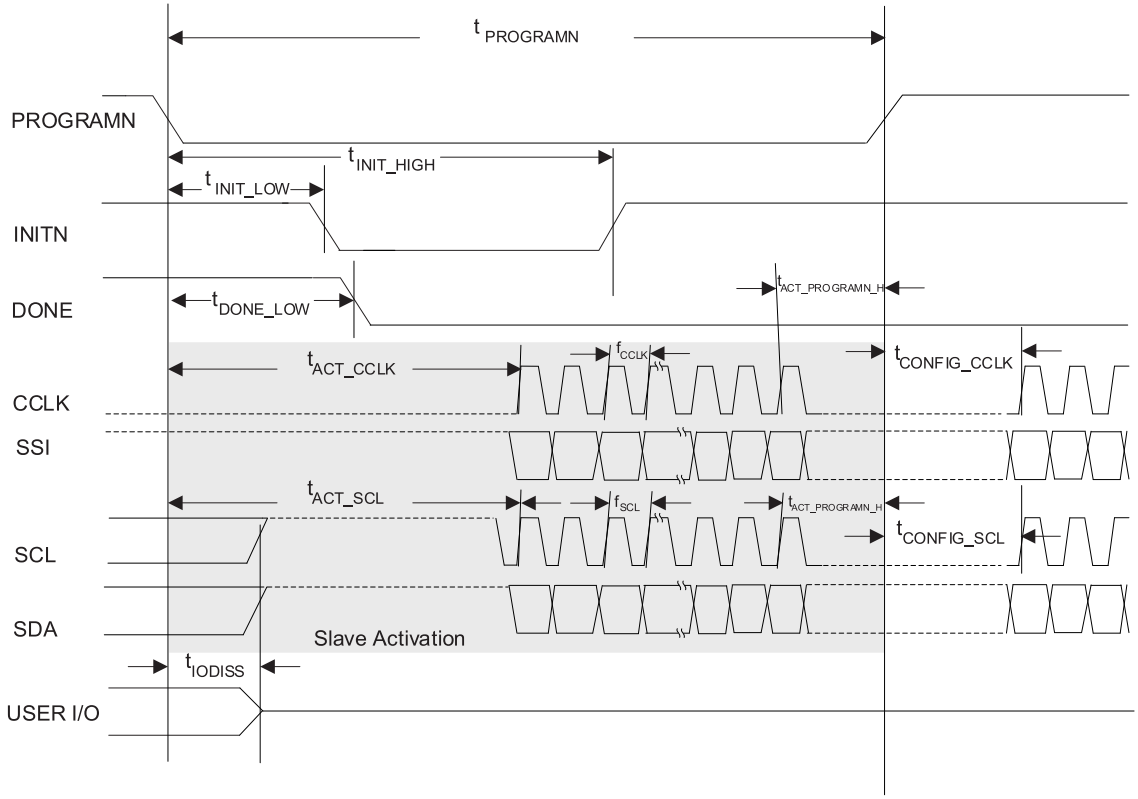


Figure 3.17. Slave SPI/I²C/I3C PROGRAMN Timing

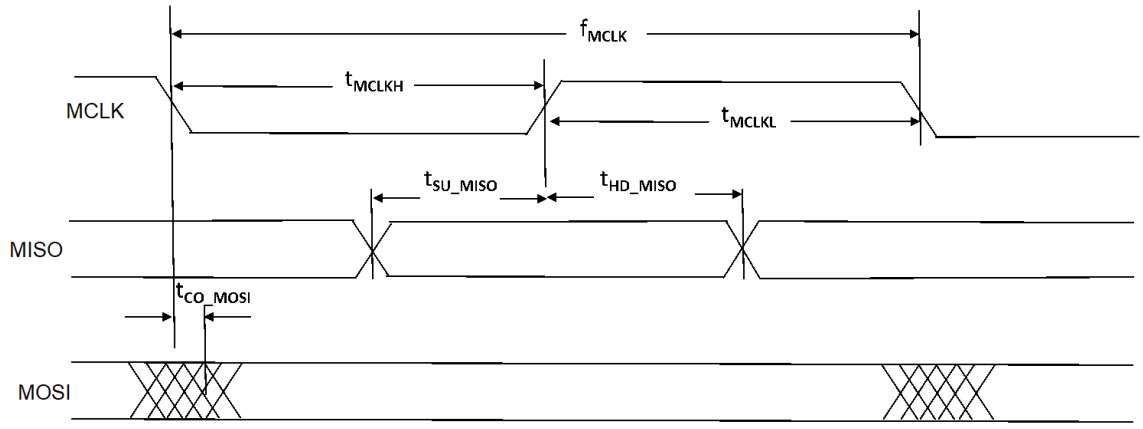


Figure 3.18. Master SPI Configuration Timing

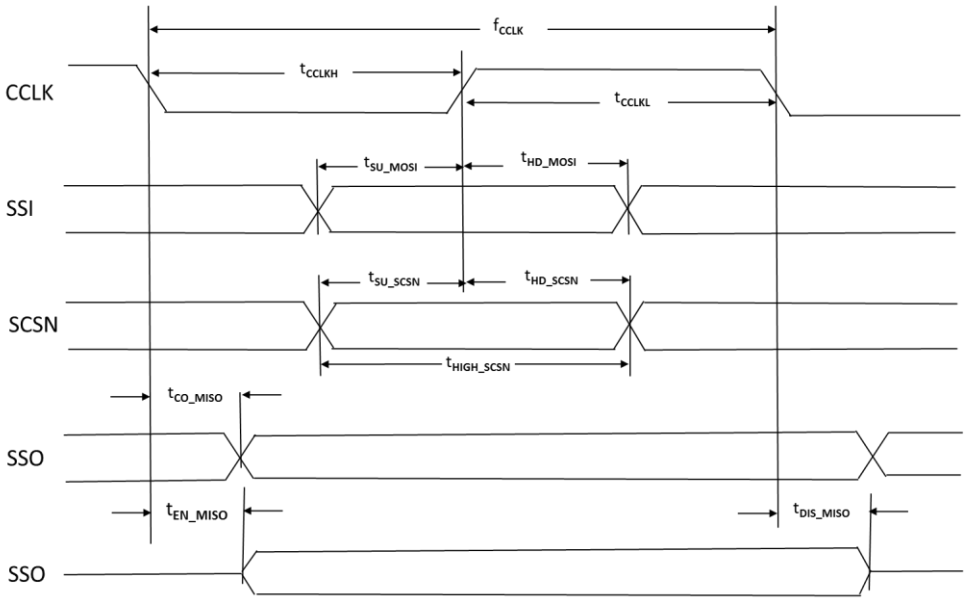


Figure 3.19. Slave SPI Configuration Timing

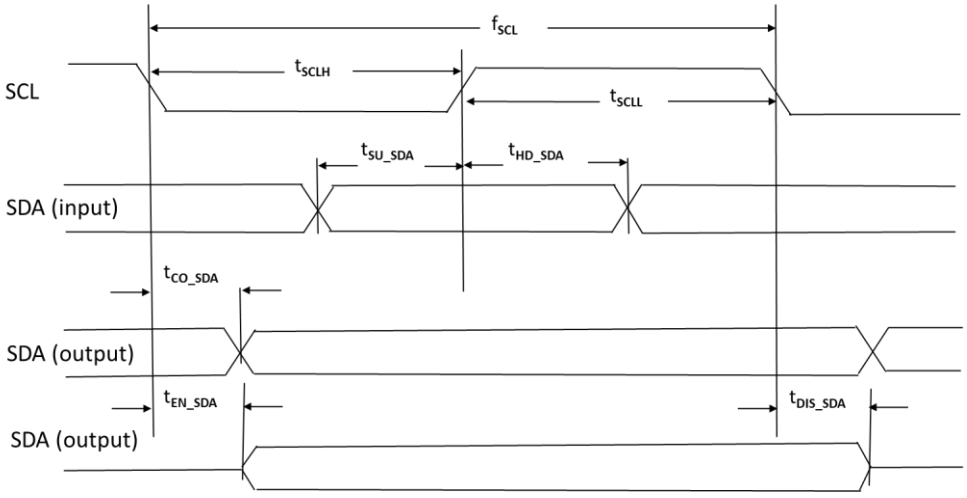


Figure 3.20. I²C /I3C Configuration Timing

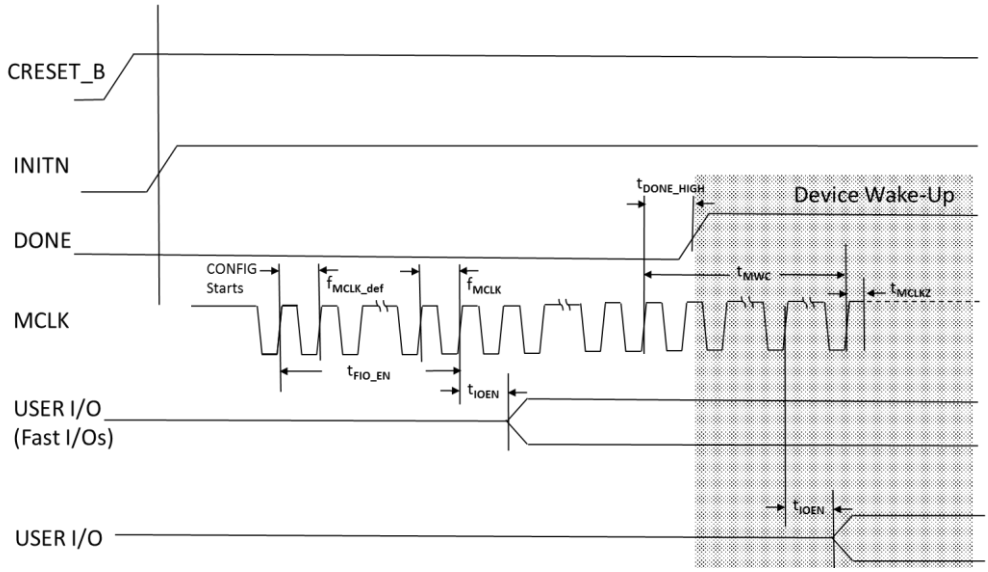


Figure 3.21. Master SPI Wake-Up Timing

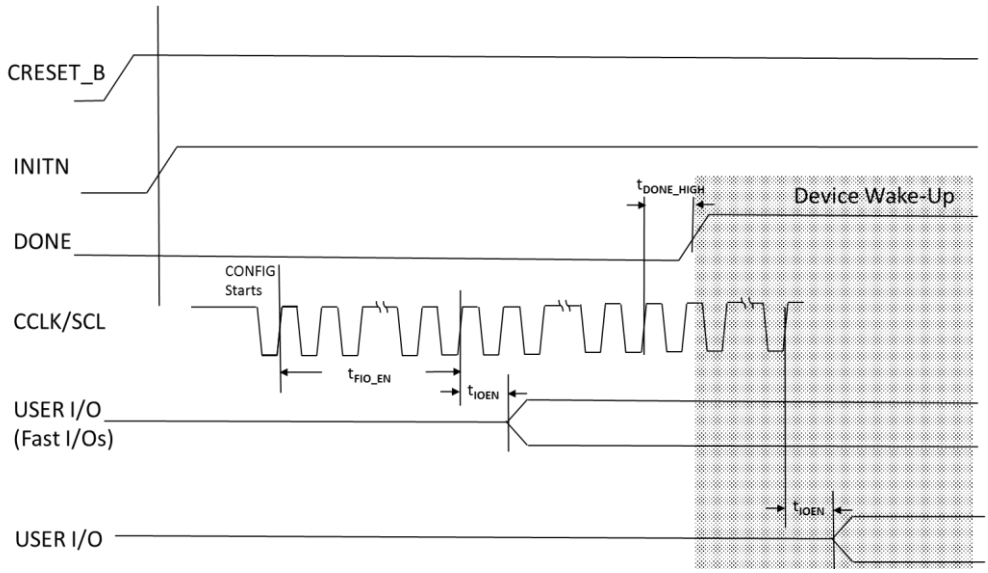


Figure 3.22. Slave SPI/I²C/I3C Wake-Up Timing

3.28. JTAG Port Timing Specifications

Over recommended operating conditions.

Table 3.47. JTAG Port Timing Specifications

Symbol	Parameter	Min	Typ.	Max	Units
f_{MAX}	TCK clock frequency	—	—	25	MHz
t_{BTCPH}	TCK clock pulse width high	20	—	—	ns
t_{BTCPL}	TCK clock pulse width low	20	—	—	ns
t_{BTS}	TCK TAP setup time	5	—	—	ns
t_{BTH}	TCK TAP hold time	5	—	—	ns
t_{BTRF}	TCK TAP rise/fall time		—	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	—	14	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	—	14	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	—	14	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	—	25	ns

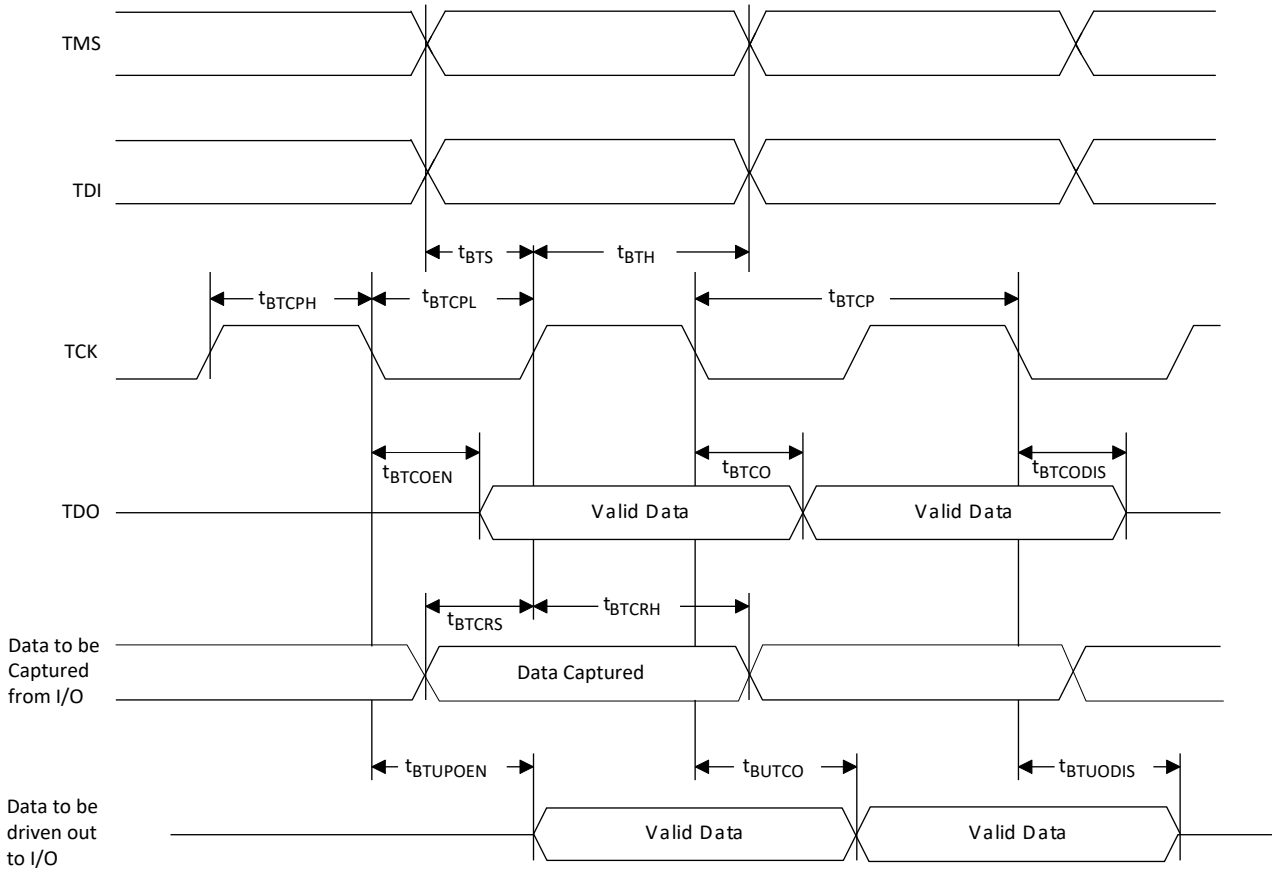
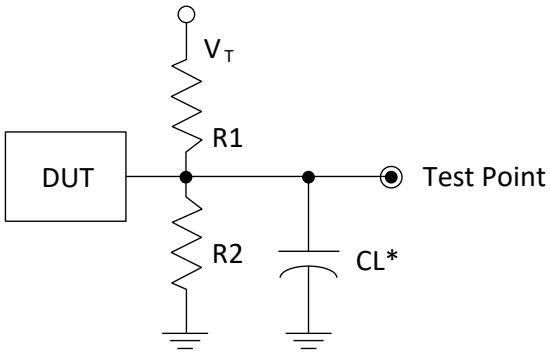


Figure 3.23. JTAG Port Timing Waveforms

3.29. Switching Test Conditions

Figure 3.24 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 3.48.



*CL Includes Test Fixture and Probe Capacitance

Figure 3.24. Output Test Load, LVTTL and LVCMOS Standards

Table 3.48. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	R_2	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L ≥ H, H ≥ L)	∞	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
				LVCMOS 2.5 = V_{CCIO}/2	—
				LVCMOS 1.8 = V_{CCIO}/2	—
				LVCMOS 1.5 = V_{CCIO}/2	—
				LVCMOS 1.2 = V_{CCIO}/2	—
LVCMOS 2.5 I/O (Z ≥ H)	∞	1 MΩ	0 pF	V_{CCIO}/2	—
LVCMOS 2.5 I/O (Z ≥ L)	1 MΩ	∞	0 pF	V_{CCIO}/2	V_{CCIO}
LVCMOS 2.5 I/O (H ≥ Z)	∞	100	0 pF	V_{OH} – 0.10	—
LVCMOS 2.5 I/O (L ≥ Z)	100	∞	0 pF	V_{OL} + 0.10	V_{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

4. DC and Switching Characteristics for Automotive

4.1. Absolute Maximum Ratings

Table 4.1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CC}, V_{CCECLK}	Supply Voltage	–0.5	1.10	V
V_{CCAUX}, V_{CCAUXA}, $V_{CCAUXH3}$, $V_{CCAUXH4}$, $V_{CCAUXH5}$	Supply Voltage	–0.5	1.98	V
$V_{CCIO0, 1, 2, 6, 7}$	I/O Supply Voltage	–0.5	3.63	V
$V_{CCIO3, 4, 5}$	I/O Supply Voltage	–0.5	1.98	V
$V_{CCPLL\_DPHY0, 1}$	Hardened D-PHY PLL Supply Voltage	–0.5	1.10	V
$V_{CCPLLSD0}$	SerDes Block PLL Supply Voltage	–0.5	1.98	V
$V_{CCA\_DPHY0, 1}$	Analog Supply Voltage for Hardened D-PHY	–0.5	1.98	V
$V_{CC\_DPHY0, 1}$	Digital Supply Voltage for Hardened D-PHY	–0.5	1.10	V
V_{CCSD0}	SerDes Supply Voltage	–0.5	1.10	V
$V_{CCADC18}$	ADC Block 1.8 V Supply Voltage	–0.5	1.98	V
$V_{CCAUXSD}$	SerDes and AUX Supply Voltage	–0.5	1.98	V
—	Input or I/O Voltage Applied, Bank 0, Bank 1,Bank 2, Bank 6, Bank 7	–0.5	3.63	V
—	Input or I/O Voltage Applied, Bank 3, Bank 4, Bank 5	–0.5	1.98	V
—	Voltage Applied on SerDes Pins	–0.5	1.98	V
T_A	Storage Temperature (Ambient)	–65	150	°C
T_J	Junction Temperature	—	+125	°C

Notes:

1. Stress above those listed under the *Absolute Maximum Ratings* may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. All V_{CCAUX} should be connected on PCB.

4.2. Recommended Operating Conditions[5]

Table 4.2. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
V_{CC}, V_{CCECLK}	Core Supply Voltage	V_{CC} = 1.0	0.95	1.00	1.05	V
V_{CCAUX}	Auxiliary Supply Voltage	Bank 0, Bank 1, Bank 2, Bank 6, Bank 7	1.746	1.80	1.89	V
$V_{CCAUXH3/4/5}$	Auxiliary Supply Voltage	Bank 3, Bank 4, Bank 5	1.746	1.80	1.89	V
V_{CCAUXA}	Auxiliary Supply Voltage for core logic	—	1.746	1.80	1.89	V
V_{CCIO}	I/O Driver Supply Voltage	V_{CCIO} = 3.3 V, Bank 0, Bank 1, Bank 2, Bank 6, Bank 7	3.135	3.30	3.465	V
		V_{CCIO} = 2.5 V, Bank 0, Bank 1, Bank 2, Bank 6, Bank 7	2.375	2.50	2.625	V
		V_{CCIO} = 1.8 V, All Banks	1.71	1.80	1.89	V
		V_{CCIO} = 1.5 V, All Banks[4]	1.425	1.50	1.575	V
		V_{CCIO} = 1.35 V, All Banks (For DDR3L Only)	1.2825	1.35	1.4175	V
		V_{CCIO} = 1.2 V, All Banks[4]	1.14	1.20	1.26	V
		V_{CCIO} = 1.0 V, Bank 3, Bank 4, Bank 5	0.95	1.00	1.05	V
D-PHY External Power Supplies						
$V_{CCA\_D\text{-}PHY}$	D-PHY Analog Power Supply	—	1.71	1.80	1.89	V
$V_{CC\_D\text{-}PHY}$	D-PHY Digital Power Supply	—	0.95	1.00	1.05	V
$V_{CCPLL\_D\text{-}PHY}$	D-PHY PLL Power Supply	—	0.95	1.00	1.05	V
ADC External Power Supplies						
$V_{CCADC18}$	ADC 1.8 V Power Supply	—	1.71	1.80	1.89	V
SerDes Block External Power Supplies						
V_{CCSD0}	Supply Voltage for SerDes Block and SerDes I/O	—	0.95	1.00	1.05	V
$V_{CCPLLSD0}$	SerDes Block PLL Supply Voltage	—	1.71	1.80	1.89	V
$V_{CCAUXSD}$	SerDes Block Auxiliary Supply Voltage	—	1.71	1.80	1.89	V
Operating Temperature						
t_{AUTO}	Junction Temperature, Automotive Operation	—	–40	—	125	°C

Notes:

1. For correct operation, all supplies must be held in their valid operation voltage range.
2. All supplies with same voltage should be from the same voltage source. Proper isolation filters are needed to properly isolate noise from each other.
3. Common supply rails must be tied together except SerDes.
4. MSPI (Bank0) and JTAG, SSPI, I^2C, and I3C (Bank 1) ports are supported for V_{CCIO} = 1.8 V to 3.3 V.
5. Data in this section is in preliminary state, subject to change.

5. Pinout Information

5.1. Signal Descriptions

Signal Name	Bank	Type	Description
Power and GND			
Vss	—	GND	Ground for internal FPGA logic and I/O
$V_{SSA\_D\text{-}PHY}$	—	GND	Analog Ground for D-PHY blocks
V_{SSSD}	—	GND	Ground for SerDes blocks
V_{CC}	—	Power	Power supply pins for core logic. V_{CC} is connected to 1.0 V (nom.) supply voltage. Power On Reset (POR) monitors this supply voltage.
V_{CCAUXA}	—	Power	Auxiliary power supply pin for internal analog circuitry. This supply is connected to 1.8 V (nom.) supply voltage. POR monitors this supply voltage.
V_{CCAUX}	—	Power	Auxiliary power supply pin for I/O Bank 0, Bank 1, Bank 2, Bank 6, and Bank 7. This supply is connected to 1.8 V (nom.) supply voltage, and is used for generating stable drive current for the I/O.
$V_{CCAUXHx}$	—	Power	Auxiliary power supply pin for I/O Bank 3, Bank 4, and Bank 5. This supply is connected to 1.8 V (nom.) supply voltage, and is used for generating stable current for the differential input comparators.
V_{CCIOx}	0-7	Power	Power supply pins for I/O bank x. For x = 0, 1, 2, 6, and 7, VCCIO can be connected to (nom.) 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V. For x = 3, 4, and 5, VCCIO can be connected to (nom.) 1.0 V, 1.2 V, 1.35 V, 1.5 V, or 1.8 V. There are dedicated and shared configuration pins in banks 0 and 1. POR monitors these banks supply voltages.
$V_{CC\_D\text{-}PHYx}$	—	Power	1.0 V (nom.) digital power supply for the hardened D-PHY blocks. X = 0, 1
$V_{CCA\_D\text{-}PHYx}$	—	Power	1.8 V (nom.) analog power supply for the hardened D-PHY blocks. X = 0, 1
$V_{CCPLL\_D\text{-}PHYx}$	—	Power	1.0 V (nom.) power supply for the hardened D-PHY blocks. X = 0, 1
$V_{CCADC18}$	—	Power	1.8 V (nom.) power supply for the ADC block.
V_{CCSD0}	—	Power	1.0 V (nom.) power supply for the SerDes block.
$V_{CCPLLSD0}$	—	Power	1.8 V (nom.) power supply for the PLL in the SerDes block.
$V_{CCAUXSD}$	—	Power	1.8 V (nom.) auxiliary power supply for the SerDes block.
Dedicated Pins			
Dedicated Configuration I/O Pin			
JTAG_EN	1	Input	LVCMOS input pin. This input selects the JTAG shared GPIO to be used for JTAG 0 = GPIO 1 = JTAG

Dedicated ADC I/O Pins			
ADC_REF[0, 1]	—	Input	ADC reference voltage, for each of the 2 ADC converters
ADC_DP/N[0, 1]	—	Input	Dedicated ADC input pairs, for each of the 2 ADC converters
Dedicated High Speed I/O Pins			
SD0_RXDP/N	—	Input	High Speed Data Differential Input Pairs
SD0_TXDP/N	—	Output	High Speed Data Differential Output Pairs
SD0_REFCLKP/N	—	Input	High Speed Reference Clock Differential Input Pairs
SD0_REXT	—	Input	High Speed External Reference Resistor Input. Resistor connects between to this pin and SD0_REFRET pin. This is used to adjust the on-chip differential termination impedance, based on the external resistance value: R_{EXT} = 909 Ω, R_{DIFF} = 80 Ω R_{EXT} = 976 Ω, R_{DIFF} = 85 Ω R_{EXT} = 1.02 kΩ, R_{DIFF} = 90 Ω R_{EXT} = 1.15 kΩ, R_{DIFF} = 100 Ω
SD0_REFRET	—	Input	High Speed Reference Return Input. These pins should be AC coupled to the VCCPLLSD0 supply
Dedicated D-PHY I/O Pins			
D-PHY[0-1]_DP/N[0-3]	—	Input, Output	Hardened D-PHY Data Input/Output Pairs, for each of the 4 High Speed lanes in the 2 Hardened D-PHY Blocks
D-PHY[0-1]_CKP/N	—	Input	Hardened D-PHY Clock Input Pairs, for each of the 2 Hardened D-PHY
Misc Pins			
NC		—	No connect.
RESERVED		—	This pin is reserved and should not be connected to anything on the
General Purpose I/O Pins			
P[T/B/L/R] [Number]_[A/B]	T = 0 R = 1, 2 B = 3, 4, 5 L = 6. 7	Input, Output, Bi-Dir	Programmable User I/O: [T/B/L/R] indicates the package pin/ball is in T (Top), B (Bottom), L (Left), or R (Right) edge of the device. [Number] identifies the PIO [A/B] pair. [A/B] shows the package pin/ball is A or B signal in the pair. PIO A and PIO B are grouped as a pair. Each A/B pair in the bottom banks supports true differential input and output buffers. When configured as differential input, differential termination of 100 Ω can be selected. Each A/B pair in the top, left and right banks does not support true differential input or output buffer. It supports all single-ended inputs and outputs, and can be used for emulated differential output buffer. Some of these user-programmable I/O are used during configuration, depending on the configuration mode. You need to make appropriate connection on the board to isolate the 2 different functions before/after configuration. Some of these user-programmable I/O are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/O for user logic. During configuration the user-programmable I/O are tristated with an internal weak pull-down resistor enabled. If any pin is not used (or not bonded to a package pin), it is tristated and default to have weak pull-down enabled after configuration.

Shared Configuration Pins[1, 2]

1. **These pins can be used for configuration during configuration mode. When configuration is completed, these pins can be used as GPIO, or shared function in GPIO. When these pins are used in dual function, you need to isolate the signal paths for the dual functions on the board.**
2. **The pins used are defined by the configuration modes detected. Slave SPI or I²C/I3C modes are detected during slave activation. Pins that are not used in the configuration mode selected are tristated during configuration, and can connect directly as GPIO in user's function.**

PRxxx /SDA/USER_SDA	1	Input, Output, Bi-Dir	Configuration: I²C/I3C Mode: SDA signal User Mode: PRxxx: GPIO User_SDA: SDA signal for I²C/I3C interface
PRxxx /SCL/USER_SCL	1	Input, Output, Bi-Dir	Configuration: I²C/I3C Mode: SCL signal User Mode: PRxxx: GPIO User_SDA: SCL signal for I²C/I3C interface
PRxxx/TDO/SSO	1	Input, Output, Bi-Dir	Configuration: Slave SPI Mode: Slave Serial Output User Mode: PRxxx: GPIO TDO: When JTAG_EN = 1, used as TDO signal for JTAG
PRxxx/TDI/SSI	1	Input, Output, Bi-Dir	Configuration: Slave SPI Mode: Slave Serial Input User Mode: PRxxx: GPIO TDI: When JTAG_EN = 1, used as TDI signal for JTAG
PRxxx/TMS/SCSN	1	Input, Output, Bi-Dir	Configuration: Slave SPI Mode: Slave Chip Select User Mode: PRxxx: GPIO TMS: When JTAG_EN = 1, used as TMS signal for JTAG
PRxxx/TCK/SCLK	1	Input, Output, Bi-Dir	Configuration: Slave SPI Mode: Slave Clock Input User Mode: PRxxx: GPIO TCK: When JTAG_EN = 1, used as TCK signal for JTAG
PTxxx/MCSNO	0	Input, Output, Bi-Dir	Configuration: Flow-through Daisy Chain Mode: Chip Select Output User Mode: PTxxx: GPIO
PTxxx/MD3	0	Input, Output, Bi-Dir	Configuration: Master Quad SPI Mode: I/O3 User Mode: PTxxx: GPIO
PTxxx/MD2	0	Input, Output, Bi-Dir	Configuration: Master Quad SPI Mode: I/O2 User Mode: PTxxx: GPIO

PTxxx/MSI/MD1	0	Input, Output, Bi-Dir	Configuration: Master SPI Mode: Master Serial Input Master Quad SPI Mode: I/O1 User Mode: PTxxx: GPIO
PTxxx/MSO/MD0	0	Input, Output, Bi-Dir	Configuration: Master SPI Mode: Master Serial Output Master Quad SPI Mode: I/O0 User Mode: PTxxx: GPIO
PTxxx/MCSN/PCLKT0_1	0	Input, Output, Bi-Dir	Configuration: Master SPI Mode: Master Chip Select Output User Mode: PTxxx: GPIO PCLKT0_0: Top PCLK Input
PTxxx/MCLK/PCLKT0_0	0	Input, Output, Bi-Dir	Configuration: Master SPI Mode: Master Clock Output User Mode: PTxxx: GPIO PCLKT0_1: Top PCLK Input
PTxxx/PROGRAMN	0	Input, Output, Bi-Dir	Configuration: PROGRAMN: Initiate configuration sequence when asserted LOW. User Mode: PTxxx: GPIO
PTxxx/INITN	0	Input, Output, Bi-Dir	Configuration: INITN: Open Drain I/O pin. This signal is driven to LOW when configuration sequence is started, to indicate the device is in initialization state. This signal is released after initialization is completed, and the configuration download can start. You can keep drive this signal LOW to delay configuration download to start. User Mode: PTxxx: GPIO
PTxxx/DONE	0	Input, Output, Bi-Dir	Configuration: DONE: Open Drain I/O pin. This signal is driven to LOW during configuration time. It is released to indicate the device has completed configuration. You can keep drive this signal LOW to delay the device to wake up from configuration. User Mode: PTxxx: GPIO
Shared User GPIO Pins[1, 2, 3, 4] **3. Shared User GPIO pins are pins that can be used as GPIO, or functional pins that connect directly to specific functional blocks, when device enters into User Mode.** **4. Declaring on assigning the pin as GPIO or specific functional pin is done by configuration bitstream, except JTAG pins.** **5. JTAG pins are controlled by JTAG_EN signal. When JTAG_EN = 1, the pins are used for JTAG interface. When JTAG = 0, the pins are used as GPIO or specific functional pin defined by configuration bitstream.** **6. Refer to package pin file.**			
Shared JTAG Pins			
PRxxx/TDO/ yyyy	1	Input, Output, Bi-Dir	User Mode: PRxxx: GPIO TDO: When JTAG_EN = 1, used as TDO signal for JTAG yyyy: Other possible selectable specific functional

PRxxx/TDI/yyyy	1	Input, Output, Bi-Dir	User Mode: PRxxx: GPIO TDI: When JTAG_EN = 1, used as TDI signal for JTAG yyyy: Other possible selectable specific functional
PRxxx/TMS/ yyyy	1	Input, Output, Bi-Dir	User Mode: PRxxx: GPIO TMS: When JTAG_EN = 1, used as TMS signal for JTAG yyyy: Other possible selectable specific functional
PRxxx/TCK/ yyyy	1	Input, Output, Bi-Dir	User Mode: PRxxx: GPIO TCK: When JTAG_EN = 1, used as TCK signal for JTAG Yyyy: Other possible selectable specific functional
Shared CLOCK Pins [1] **1. Some PCLK pins can also be used as GPLL reference clock input pin. Refer to CrossLink-NX sysCLOCK PLL/DLL Design and Usage Guide (FPGA-TN-02095).**			
PBxxx/PCLK[T,C][3,4,5]_[0-3]/yyyy	3, 4, 5	Input, Output, Bi-Dir	User Mode: PBxxx: GPIO PCLK: Primary Clock or GPLL Refclk signal [T,C] = True/Complement when using differential signaling [3,4,5] = Bank [0-3] Up to 4 signals in the bank yyyy: Other possible selectable specific functional
PTxxx/PCLKT0_[0-1]/yyyy	0	Input, Output, Bi-Dir	User Mode: PTxxx: GPIO PCLKT: Primary Clock or GPLL Refclk signal (Only Single Ended) [0-1] Up to 2 signals in the bank yyyy: Other possible selectable specific functional
PRxxx/PCLKT[1,2]_[0-2]/yyyy	1, 2	Input, Output, Bi-Dir	User Mode: PRxxx: GPIO PCLKT: Primary Clock or GPLL Refclk signal (Only Single Ended) [0-2] Up to 3 signals in the bank yyyy: Other possible selectable specific functional
PLxxx/PCLKT[6,7]_[0-2]/yyyy	6, 7	Input, Output, Bi-Dir	User Mode: PLxxx: GPIO PCLKT: Primary Clock or GPLL Refclk signal (Only Single Ended) [0-2] Up to 3 signals in the bank yyyy: Other possible selectable specific functional
PBxxx/LRC_GPLL[T,C]_IN/yyyy	3	Input, Output, Bi-Dir	User Mode: PBxxx: GPIO LRC_GPLL: Lower Right GPLL Refclk signal [T,C] = True/Complement when using differential signaling yyyy: Other possible selectable specific functional
PBxxx/LLC_GPLL[T,C]_IN/yyyy	5	Input, Output, Bi-Dir	User Mode: PBxxx: GPIO LLC_GPLL: Lower Left GPLL Refclk signal [T,C] = True/Complement when using differential signaling yyyy: Other possible selectable specific functional
PLxxx/ULC_GPLLT_IN/yyyy	7	Input, Output, Bi-Dir	User Mode: PLxxx: GPIO ULC_GPLL: Upper Left GPLL Refclk signal (Only Single Ended) yyyy: Other possible selectable specific functional

PRxxx/URC_GPLLT_IN/yyyy	1	Input, Output, Bi-Dir	User Mode: PRxxx: GPIO URC_GPLL: Upper Right GPLL Refclk signal (Only Single Ended) yyyy: Other possible selectable specific functional
Shared VREF Pins			
PBxxx/VREF[3,4,5]_[1-2]/yyyy	3, 4, 5	Input, Output, Bi-Dir	User Mode: PBxxx: GPIO VREF: Reference Voltage for DDR memory function [3,4,5] = Bank [1-2] Up to VREFs for each bank yyyy: Other possible selectable specific functional
Shared ADC Pins			
PBxxx/ADC_C[P,N]nn/yyyy	3, 4, 5	Input, Output, Bi-Dir	User Mode: PBxxx: GPIO ADC_C: ADC Channel Inputs [P,N] = Positive or Negative Input nn = ADC Channel number (0 – 15) yyyy: Other possible selectable specific functional
Shared Comparator Pins			
PBxxx/COMP[1-3][P,N]/yyyy	3, 5	Input, Output, Bi-Dir	User Mode: PBxxx: GPIO COMP: Differential Comparator Input [P,N] = Positive or Negative Input [1-3] = Input to Comparators 1-3 yyyy: Other possible selectable specific functional
Shared SGMII Pins			
PBxxx/SGMII_RX[P,N][0-1]/yyyy	3, 5	Input, Output, Bi-Dir	User Mode: PBxxx: GPIO SGMII_RX: Differential SGMII RX Inputs [P,N] = Positive or Negative Input [0-1] = Input to SGMII RX0 or RX1 yyyy: Other possible selectable specific functional

Note: Not all signals are available as external pins in all packages. Refer to the Pinout List file for various package details.

5.2. Pin Information Summary

5.2.1. CrossLink-NX Family

Pin Information Summary		LIFCL-17				LIFCL-40				
		72WLCSP	72 QFN	121csfBGA	256caBGA	121csfBGA	72 QFN	289csBGA	256caBGA	400caBGA
User I/O Pins										
General Purpose Inputs/Outputs per Bank	Bank 0	8	11	12	12	12	10	12	12	12
	Bank 1	7	7	11	11	11	7	19	20	21
	Bank 2	—	—	—	—	—	—	24	13	28
	Bank 3	12	12	16	16	16	12	32	32	32
	Bank 4	—	—	16	16	22	—	32	32	32
	Bank 5	12	10	16	16	10	10	10	10	10
	Bank 6	—	—	—	—	—	—	28	26	28
	Bank 7	—	—	—	—	—	—	16	11	22
Total Single-Ended User I/O		39	40	71	71	71	39	173	156	185
Differential Input / Output Pairs	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0
	Bank 2	0	0	0	0	0	0	0	0	0
	Bank 3	12	12	16	16	16	12	32	32	32
	Bank 4	—	—	16	16	22	—	32	32	32
	Bank 5	12	10	16	16	10	10	10	10	10
	Bank 6	0	0	0	0	0	0	0	0	0
	Bank 7	0	0	0	0	0	0	0	0	0
Total Differential I/O		24	22	48	48	48	22	74	74	74
Power Pins										
V_{CC}, V_{CCECLK}		3	8	3	5	3	8	6	5	8
V_{CCAUXA}		—	—	—	—	—	—	1	1	1
V_{CCAUX}		2	2	1	3	1	2	2	2	3
$V_{CCAUXHx}$		2	2	3	3	3	2	3	3	3
$V_{CCAUXSD}$		—	—	—	—	—	—	1	1	1
V_{CCIO}	Bank 0	1	1	1	1	1	1	1	1	1
	Bank 1	1	1	1	1	1	1	2	1	2
	Bank 2	—	—	—	—	—	—	2	1	2
	Bank 3	1	2	1	1	1	2	2	1	2
	Bank 4	—	—	1	1	1	—	2	1	2
	Bank 5	1	1	1	1	1	1	1	1	1
	Bank 6	—	—	—	—	—	—	2	1	2
	Bank 7	—	—	—	—	—	—	2	1	2
$V_{CC\_D\text{-}PHYx}$		1	2	2	2	2	2	2	2	2
$V_{CCA\_D\text{-}PHYx}$		1	1	2	2	2	1	2	2	2
$V_{CCPLL\_D\text{-}PHYx}$		1	1	2	2	2	1	2	2	2
V_{CCSD0}		—	—	—	—	—	—	2	1	2
$V_{CCPLLSD0}$		—	—	—	—	—	—	1	1	1
$V_{CCADC18}$		—	1	—	1	—	1	1	1	1
Total Power Pins		14	22	18	23	18	22	37	29	40

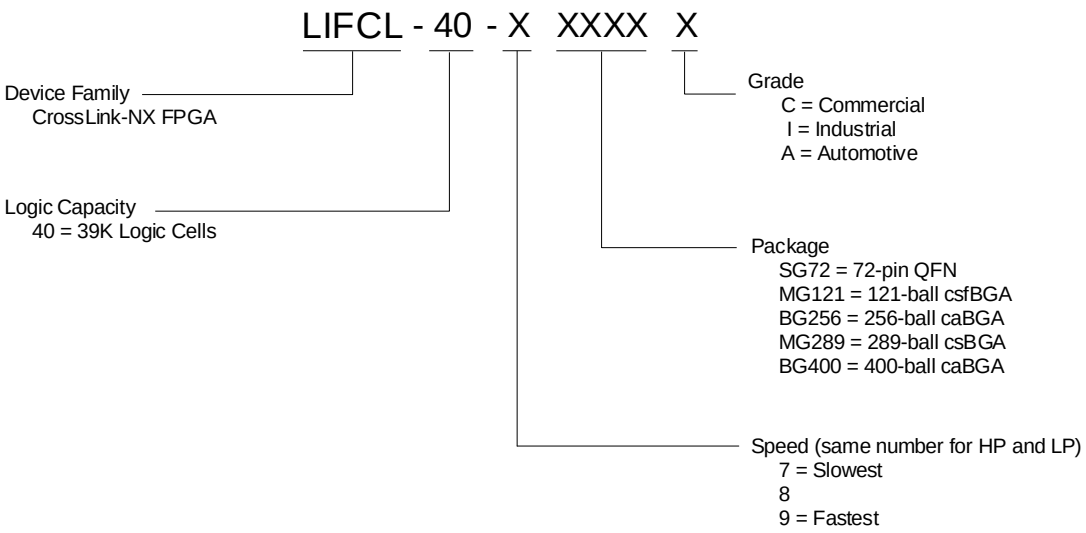
Pin Information Summary		LIFCL-17				LIFCL-40				
		72WLCSP	72 QFN	121csfBGA	256caBGA	121csfBGA	72 QFN	289csBGA	256caBGA	400caBGA
GND Pins										
Vss		5	—	6	20	6	—	26	22	37
V_{SSADC}		—	—	—	1	—	—	1	1	1
V_{SSSD}		—	—	—	—	—	—	8	5	12
$V_{SSA\_D\text{-}PHY}$		3	—	5	8	5	—	9	8	7
Total GND Pins		8	—	11	29	11	—	44	36	57
Dedicated Pins										
Dedicated ADC Channels (pairs)		—	—	—	2	—	—	—	—	0
Dedicated ADC Reference Voltage Pins		—	—	—	2	—	—	—	—	0
Dedicated D-PHY Data Channels (pairs)		4	4	8	8	8	4	8	8	8
Dedicated D-PHY Clock (pairs)		1	1	2	2	2	1	2	2	2
Dedicated Misc Pins										
JTAGEN		1	1	1	1	1	1	1	1	1
NC		—	—	—	106	—	—	—	—	
RESERVED		—	—	—	—	—	—	—	—	
Total Dedicated Pins		11	11	21	133	11	6	11	11	11
Shared Pins										
Shared Configuration Pins	Bank 0	8	10	10	10	10	10	10	10	10
	Bank 1	—	—	—	—	6	6	6	6	6
	Bank 2	0	0	0	0	0	0	0	0	0
	Bank 3	0	0	0	0	0	0	0	0	0
	Bank 4	0	0	0	0	0	0	0	0	0
	Bank 5	0	0	0	0	0	0	0	0	0
	Bank 6	0	0	0	0	0	0	0	0	0
	Bank 7	0	0	0	0	0	0	0	0	0
Shared JTAG Pins	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	4	4	4	4	4	4	4	4	4
	Bank 2	0	0	0	0	0	0	0	0	0
	Bank 3	0	0	0	0	0	0	0	0	0
	Bank 4	0	0	0	0	0	0	0	0	0
	Bank 5	0	0	0	0	0	0	0	0	0
	Bank 6	0	0	0	0	0	0	0	0	0
	Bank 7	0	0	0	0	0	0	0	0	0
Shared PCLK Pins	Bank 0	—	—	2	2	2	2	2	2	2
	Bank 1	—	—	3	3	3	—	3	3	3
	Bank 2	—	—	—	—	—	—	3	3	3
	Bank 3	8	8	8	8	8	8	8	8	8
	Bank 4	—	—	8	8	8	—	8	8	8
	Bank 5	8	8	8	8	8	8	8	8	8
	Bank 6	—	—	—	—	—	—	3	3	3
	Bank 7	—	—	—	—	—	—	3	3	3

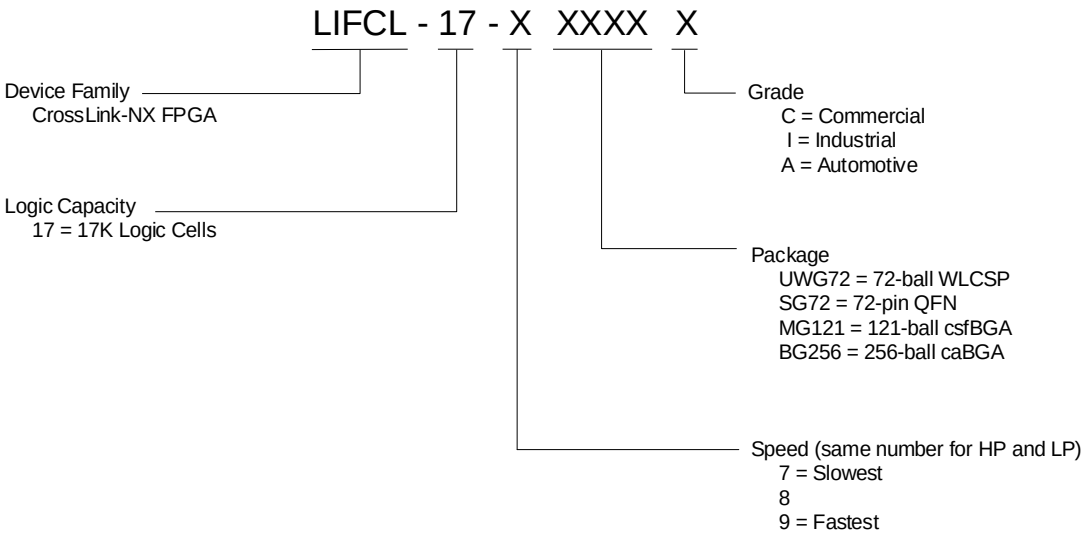
Pin Information Summary		LIFCL-17				LIFCL-40				
		72WLCSP	72 QFN	121csfBGA	256caBGA	121csfBGA	72 QFN	289csBGA	256caBGA	400caBGA
Shared GPLL Pins	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	—	—	—	—	—	—	—	—	0
	Bank 2	0	0	0	0	0	0	0	0	0
	Bank 3	2	2	2	2	2	2	2	2	2
	Bank 4	—	—	—	—	—	—	—	—	0
	Bank 5	2	2	2	2	2	2	2	2	2
	Bank 6	0	0	0	0	0	0	0	0	0
	Bank 7	—	—	—	—	—	—	2	2	2
Shared VREF Pins	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0
	Bank 2	0	0	0	0	0	0	0	0	0
	Bank 3	2	2	2	2	2	2	2	2	2
	Bank 4	—	—	2	2	1	—	2	2	2
	Bank 5	2	2	2	2	2	2	2	2	2
	Bank 6	0	0	0	0	0	0	0	0	0
	Bank 7	0	0	0	0	0	0	0	0	0
Shared ADC Channels (pairs)	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0
	Bank 2	0	0	0	0	0	0	0	0	0
	Bank 3	5	5	7	7	7	5	12	12	12
	Bank 4	—	—	—	—	—	—	—	—	0
	Bank 5	4	4	4	4	4	4	4	4	4
	Bank 6	0	0	0	0	0	0	0	0	0
	Bank 7	0	0	0	0	0	0	0	0	0
Shared Comparator Channels (pairs)	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0
	Bank 2	0	0	0	0	0	0	0	0	0
	Bank 3	—	—	—	—	—	—	2	2	3
	Bank 4	—	—	—	—	—	—	—	—	0
	Bank 5	3	3	3	3	3	3	3	3	3
	Bank 6	0	0	0	0	0	0	0	0	0
	Bank 7	0	0	0	0	0	0	0	0	0
Shared SGMII Channels (pairs)	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0
	Bank 2	0	0	0	0	0	0	0	0	0
	Bank 3	—	—	—	—	—	—	—	—	0
	Bank 4	0	0	0	0	0	0	0	0	0
	Bank 5	2	2	2	2	2	2	2	2	2
	Bank 6	0	0	0	0	0	0	0	0	0
	Bank 7	0	0	0	0	0	0	0	0	0

6. Ordering Information

Lattice provides a wide variety of services for its products including custom marking, factory programming, known good die, and application specific testing. Contact your local sales representatives for more details.

6.1. CrossLink-NX Part Number Description





6.2. Ordering Part Numbers

6.2.1. Commercial

Part Number	Speed	Package	Pins	Temp.	Logic Cells (K)
LIFCL-17-8UWG72C	–8	Lead free WLCSP	72	Commercial	17
LIFCL-17-7SG72C	–7	Lead free QFN	72	Commercial	17
LIFCL-17-8SG72C	–8	Lead free QFN	72	Commercial	17
LIFCL-17-9SG72C	–9	Lead free QFN	72	Commercial	17
LIFCL-17-7MG121C	–7	Lead free csfBGA	121	Commercial	17
LIFCL-17-8MG121C	–8	Lead free csfBGA	121	Commercial	17
LIFCL-17-9MG121C	–9	Lead free csfBGA	121	Commercial	17
LIFCL-17-7BG256C	–7	Lead free caBGA	256	Commercial	17
LIFCL-17-8BG256C	–8	Lead free caBGA	256	Commercial	17
LIFCL-17-9BG256C	–9	Lead free caBGA	256	Commercial	17
LIFCL-40-7SG72C	–7	Lead free QFN	72	Commercial	39
LIFCL-40-8SG72C	–8	Lead free QFN	72	Commercial	39
LIFCL-40-9SG72C	–9	Lead free QFN	72	Commercial	39
LIFCL-40-7MG121C	–7	Lead free csfBGA	121	Commercial	39
LIFCL-40-8MG121C	–8	Lead free csfBGA	121	Commercial	39
LIFCL-40-9MG121C	–9	Lead free csfBGA	121	Commercial	39
LIFCL-40-7MG289C	–7	Lead free csBGA	289	Commercial	39
LIFCL-40-8MG289C	–8	Lead free csBGA	289	Commercial	39
LIFCL-40-9MG289C	–9	Lead free csBGA	289	Commercial	39
LIFCL-40-7BG256C	–7	Lead free caBGA	256	Commercial	39
LIFCL-40-8BG256C	–8	Lead free caBGA	256	Commercial	39
LIFCL-40-9BG256C	–9	Lead free caBGA	256	Commercial	39
LIFCL-40-7BG400C	–7	Lead free caBGA	400	Commercial	39
LIFCL-40-8BG400C	–8	Lead free caBGA	400	Commercial	39
LIFCL-40-9BG400C	–9	Lead free caBGA	400	Commercial	39

6.2.2. Industrial

Part Number	Speed	Package	Pins	Temp.	Logic Cells (K)
LIFCL-17-8UWG72I	–8	Lead free WLCSP	72	Industrial	17
LIFCL-17-7SG72I	–7	Lead free QFN	72	Industrial	17
LIFCL-17-8SG72I	–8	Lead free QFN	72	Industrial	17
LIFCL-17-9SG72I	–9	Lead free QFN	72	Industrial	17
LIFCL-17-7MG121I	–7	Lead free csfBGA	121	Industrial	17
LIFCL-17-8MG121I	–8	Lead free csfBGA	121	Industrial	17
LIFCL-17-9MG121I	–9	Lead free csfBGA	121	Industrial	17
LIFCL-17-7BG256I	–7	Lead free caBGA	256	Industrial	17
LIFCL-17-8BG256I	–8	Lead free caBGA	256	Industrial	17
LIFCL-17-9BG256I	–9	Lead free caBGA	256	Industrial	17
LIFCL-40-7SG72I	–7	Lead free QFN	72	Industrial	39
LIFCL-40-8SG72I	–8	Lead free QFN	72	Industrial	39
LIFCL-40-9SG72I	–9	Lead free QFN	72	Industrial	39
LIFCL-40-7MG121I	–7	Lead free csfBGA	121	Industrial	39
LIFCL-40-8MG121I	–8	Lead free csfBGA	121	Industrial	39
LIFCL-40-9MG121I	–9	Lead free csfBGA	121	Industrial	39

Part Number	Speed	Package	Pins	Temp.	Logic Cells (K)
LIFCL-40-7MG289I	–7	Lead free csBGA	289	Industrial	39
LIFCL-40-8MG289I	–8	Lead free csBGA	289	Industrial	39
LIFCL-40-9MG289I	–9	Lead free csBGA	289	Industrial	39
LIFCL-40-7BG256I	–7	Lead free caBGA	256	Industrial	39
LIFCL-40-8BG256I	–8	Lead free caBGA	256	Industrial	39
LIFCL-40-9BG256I	–9	Lead free caBGA	256	Industrial	39
LIFCL-40-7BG400I	–7	Lead free caBGA	400	Industrial	39
LIFCL-40-8BG400I	–8	Lead free caBGA	400	Industrial	39
LIFCL-40-9BG400I	–9	Lead free caBGA	400	Industrial	39

6.2.3. Automotive

Part Number	Speed	Package	Pins	Temp.	Logic Cells (K)
LIFCL-17-7MG121A	–7	Lead free csfBGA	121	Automotive	17
LIFCL-17-7BG256A	–7	Lead free caBGA	256	Automotive	17
LIFCL-40-7MG121A	–7	Lead free csfBGA	121	Automotive	39
LIFCL-40-7BG256A	–7	Lead free caBGA	256	Automotive	39

Supplemental Information

For Further Information

A variety of technical notes for the CrossLink-NX family are available.

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL) – www.jedec.org
- PCI – www.pcisig.com

Revision History

Revision 1.0, April 2021

Section	Change Summary
All	Production release

www.latticesemi.com